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DATA ACQUISITION

NEW RELEASES

1992

HARRIS SEMICONDUCTOR

$5.00

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DATA ACQUISITION NEW PRODUCTS

This supplementary data book contains specifications for new products released since the main Data Acquisition data book last printed in 1991. Included in this supplementary data book is a listing of all products described in the main data book. For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG-201S; ordering information below.)

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DATA ACQUISITION NEW PRODUCTS
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HARRIS SEMICONDUCTOR

DATA ACQUISITION NEW PRODUCTS 1

GENERAL INFORMATION

1

DATA ACQUISITION

NEW PRODUCTS

Other Data Acquisition Products Contained in Main Data Acquisition Data Book (DB301.1)

AD590	2-Wire Current Output Temperature Transducer
AD7520	10-Bit Multiplying D/A Converter
AD7521	12-Bit Multiplying D/A Converter
AD7523	8-Bit Multiplying D/A Converter
AD7530	10-Bit Multiplying D/A Converter
AD7531	12-Bit Multiplying D/A Converter
AD7533	10-Bit Multiplying D/A Converter
AD7541	12-Bit Multiplying D/A Converter
AD7545	12-Bit Buffered Multiplying CMOS DAC
ADC0802	8-Bit µP-Compatible A/D Converter
ADC0803	8-Bit µP-Compatible A/D Converter
ADC0804	8-Bit µP-Compatible A/D Converter
CA3161	BCD to Seven Segment Decoder/Driver
CA3304	CMOS Video-Speed 4-Bit Flash A/D Converter
CA3306	CMOS Video-Speed 6-Bit Flash A/D Converter
CA3310/CA3310A	CMOS 10-Bit A/D Converter with Internal Track and Hold
CA3318C	CMOS Video-Speed 8-Bit Flash A/D Converter
CA3338	CMOS Video-Speed 8-Bit R-2R D/A Converter
DG180	Dual SPST 10 Ohm High-Speed Driver with JFET Switch
DG181	Dual SPST 30 Ohm High-Speed Driver with JFET Switch
DG182	Dual SPST 75 Ohm High-Speed Driver with JFET Switch
DG183	Dual DPST 10 Ohm High-Speed Driver with JFET Switch
DG184	Dual DPST 30 Ohm High-Speed Driver with JFET Switch
DG185	Dual DPST 75 Ohm High-Speed Driver with JFET Switch
DG186	SPDT 10 Ohm High-Speed Driver with JFET Switch
DG187	SPDT 30 Ohm High-Speed Driver with JFET Switch
DG188	SPDT 75 Ohm High-Speed Driver with JFET Switch
DG189	Dual SPDT 10 Ohm High-Speed Driver with JFET Switch
DG190	Dual SPDT 30 Ohm High-Speed Driver with JFET Switch
DG191	Dual SPDT 75 Ohm High-Speed Driver with JFET Switch
DG200	Dual SPST CMOS Analog Switch
DG201	Quad SPST CMOS Analog Switch
DG201A	Quad Monolithic SPST CMOS Analog Switch
DG202	Quad Monolithic SPST CMOS Analog Switch
DG211	Quad Monolithic SPST CMOS Analog Switch
DG212	Quad Monolithic SPST CMOS Analog Switch

Other Data Acquisition Products Contained in Main Data Acquisition Data Book (DB301.1) (Continued)

DG300A	Dual SPST TTL Compatible CMOS Analog Switch
DG301A	SPDT TTL Compatible CMOS Analog Switch
DG302A	Dual DPST TTL Compatible CMOS Analog Switch
DG303A	Dual SPDT TTL Compatible CMOS Analog Switch
DG308A	Quad Monolithic SPST CMOS Analog Switch
DG309	Quad Monolithic SPST CMOS Analog Switch
DG506A	16-Channel CMOS Analog Multiplexer.
DG507A	Dual 8-Channel CMOS Analog Multiplexer
DG508A	8-Channel CMOS Analog Multiplexer
DG509A	Dual 4-Channel CMOS Analog Multiplexer
DG526	16-Channel CMOS Latchable Multiplexer
DG527	Dual 8-Channel CMOS Latchable Multiplexer
DG528	8-Channel Latchable Multiplexer
DG529	Dual 4-Channel Latchable Multiplexer
HI-200	Dual SPST CMOS Analog Switch
HI-201	Quad SPST CMOS Analog Switch
HI-201HS	High-Speed Quad SPST CMOS Analog Switch.
HI-222	High Frequency Video Switch
HI-300	Dual SPST CMOS Analog Switch
HI-301	SPDT CMOS Analog Switch
HI-302	Dual DPST CMOS Analog Switch
HI-303	Dual SPDT CMOS Analog Switch
HI-304	Dual SPST CMOS Analog Switch
HI-305	SPDT CMOS Analog Switch
HI-306	Dual DPST CMOS Analog Switch
HI-307	Dual SPDT CMOS Analog Switch
HI-381	Dual SPST CMOS Analog Switch
HI-384	Dual DPST CMOS Analog Switch
HI-387	SPDT CMOS Analog Switch
HI-390	Dual SPDT CMOS Analog Switch
HI-506	Single 16-Channel CMOS Analog Multiplexer
HI-506A	Single 16-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-507	Differential 8-Channel CMOS Analog Multiplexer
HI-507A	Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-508	Single 8-Channel CMOS Analog Multiplexer
HI-508A	Single 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection.

Other Data Acquisition Products Contained in Main Data Acquisition Data Book (DB301.1) (Continued)

HI-509	Differential 4-Channel CMOS Analog Multiplexer
HI-509A	Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-516	Programmable 16-Channel/Differential 8-Channel CMOS High-Speed Analog Multiplexer
HI-518	Programmable 8-Channel/Differential 4-Channel CMOS High-Speed Analog Multiplexer
HI-524	4-Channel Wideband and Video Multiplexer
HI-539	Monolithic, 4-Channel, Low Level, Differential Multiplexer
HI-546	Single 16-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-547	Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-548	Single 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-549	Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection
HI-562A	12-Bit High-Speed Monolithic D/A Converter
HI-565A	High-Speed Monolithic D/A Converter with Reference
HI-574A	Fast, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-674A	12µs, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-774	8µs, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-1818A	Low Resistance Single 8-Channel CMOS Analog Multiplexer
HI-1828A	Low Resistance Differential 4-Channel CMOS Analog Multiplexer
HI-5040	SPST CMOS Analog Switch
HI-5041	Dual SPST CMOS Analog Switch
HI-5042	SPDT CMOS Analog Switch
HI-5043	Dual SPDT CMOS Analog Switch
HI-5044	DPST CMOS Analog Switch
HI-5045	Dual DPST CMOS Analog Switch
HI-5046	DPDT CMOS Analog Switch
HI-5046A	DPDT CMOS Analog Switch
HI-5047	4PST CMOS Analog Switch
HI-5047A	4PST CMOS Analog Switch
HI-5048	Dual SPST CMOS Analog Switch
HI-5049	Dual DPST CMOS Analog Switch
HI-5050	SPDT CMOS Analog Switch
HI-5051	Dual SPDT CMOS Analog Switch
HI-5700	8-Bit, 20MSPS Flash A/D Converter
HI-5701	6-Bit, 30MSPS Flash A/D Converter
HI-7151	10-Bit High-Speed A/D Converter with Track and Hold
HI-7152	10-Bit High-Speed A/D Converter with Track and Hold
HI-7153	8-Channel 10-Bit High Speed Sampling A/D Converter

Other Data Acquisition Products Contained in Main Data Acquisition Data Book (DB301.1) (Continued)

HI-7159A	Microprocessor Compatible 5 1/2-Digit A/D Converter
HI-DAC80V	12-Bit, Low Cost Monolithic D/A Converter
HI-DAC85V	12-Bit, Low Cost Monolithic D/A Converter
ICL232	+5 Volt Powered Dual RS-232 Transmitter/Receiver
ICL71C03/ICL8052	Precision 4 1/2-Digit A/D Converter
ICL71C03/ICL8068	Precision 4 1/2-Digit A/D Converter
ICL7104/ICL8052	14/16-Bit µP-Compatible 2-Chip A/D Converter
ICL7104/ICL8068	14/16-Bit µP-Compatible 2-Chip A/D Converter
ICL7106	3 1/2-Digit LCD Single-Chip A/D Converter
ICL7107	3 1/2-Digit LED Single-Chip A/D Converter
ICL7109	12-Bit µP-Compatible A/D Converter
ICL7115	14-Bit High-Speed CMOS µP-Compatible A/D Converter
ICL7116	3 1/2-Digit with Display Hold Single-Chip A/D Converter
ICL7117	3 1/2-Digit with Display Hold Single-Chip A/D Converter
ICL7121	16-Bit Multiplying Microprocessor-Compatible D/A Converter
ICL7126	3 1/2-Digit Low Power Single-Chip A/D Converter
ICL7129	4 1/2-Digit LCD Single-Chip A/D Converter
ICL7134	14-Bit Multiplying µP-Compatible D/A Converter
ICL7135	4 1/2-Digit BCD Output A/D Converter
ICL7136	3 1/2-Digit LCD Low Power A/D Converter
ICL7137	3 1/2-Digit LED Low Power Single-Chip A/D Converter
ICL7139	3 3/4-Digit Autoranging Multimeter
ICL7149	Low Cost 3 3/4-Digit Autoranging Multimeter
ICL8052	A/D Converter - Low Leakage, Low Noise
ICL8068	A/D Converter - Low Leakage, Low Noise
ICL8069	Low Voltage Reference
ICM7170	µP-Compatible Real-Time Clock
ICM7207/A	CMOS Timebase Generator
ICM7208	7-Digit LED Display Counter
ICM7209	Timebase Generator
ICM7211	4-Digit LCD Display Driver
ICM7212	4-Digit LED Display Driver
ICM7213	One Second/One Minute Timebase Generator
ICM7216A/B/D	8-Digit Multi-Function Frequency Counter/Timer
ICM7217	4-Digit LED Display Programmable Up/Down Counter
ICM7218	8-Digit LED Multiplexed Display Driver
ICM7224	4 1/2-Digit LCD/LED Display Counter

Other Data Acquisition Products Contained in Main Data Acquisition Data Book (DB301.1) (Continued)

ICM7226A/B	8-Digit Multi-Function Frequency Counter/Timer
ICM7228	8-Digit LED Multiplexed Display Driver
ICM7231	Numeric/Alphanumeric Triplexed LCD Display Driver
ICM7232	Numeric/Alphanumeric Triplexed LCD Display Driver
ICM7243	8-Character µP-Compatible LED Display Driver
ICM7249	5 1/2-Digit LCD µ-Power Event/Hour Meter
IH401A	Quad Varafet Analog Switch
IH5009	Quad 100 Ohm Virtual Ground Analog Switch
IH5010	Quad 150 Ohm Virtual Ground Analog Switch
IH5011	Quad 100 Ohm Virtual Ground Analog Switch
IH5012	Quad 150 Ohm Virtual Ground Analog Switch
IH5014	Triple 150 Ohm Virtual Ground Analog Switch
IH5016	Triple 150 Ohm Virtual Ground Analog Switch
IH5017	Dual 100 Ohm Virtual Ground Analog Switch
IH5018	Dual 150 Ohm Virtual Ground Analog Switch
IH5019	Dual 100 Ohm Virtual Ground Analog Switch
IH5020	Dual 150 Ohm Virtual Ground Analog Switch
IH5022	Single 150 Ohm Virtual Ground Analog Switch
IH5024	Single 150 Ohm Virtual Ground Analog Switch
IH5043	Dual SPDT 75 Ohm High-Level CMOS Analog Switch
IH5052	Quad SPST CMOS Analog Switch
IH5053	Quad SPST CMOS Analog Switch
IH5140	SPST High-Level CMOS Analog Switch
IH5141	Dual SPST High-Level CMOS Analog Switch
IH5142	SPDT High-Level CMOS Analog Switch
IH5143	Dual SPDT High-Level CMOS Analog Switch
IH5144	DPST High-Level CMOS Analog Switch
IH5145	Dual DPST High-Level CMOS Analog Switch
IH5151	Dual SPDT High-Level CMOS Analog Switch
IH5341	Dual SPST CMOS RF/Video Switch
IH5352	Quad SPST CMOS RF/Video Switch
IH6108	8-Channel CMOS Analog Multiplexer
IH6201	Dual CMOS Driver/Voltage Translator
IH6208	4-Channel Differential CMOS Analog Multiplexer
IM6654	4096-Bit CMOS UV EPROM

HARRIS SEMICONDUCTOR

DG401, DG403 DG405

Monolithic Dual CMOS Analog Switches

PRELIMINARY

July 1992

Features

- ON-Resistance < 35Ω
- Low Power Consumption (P_D < 35μW)
- Fast Switching Action
  - t_{ON} <150ns
  - t_{OFF} <100ns
- Low Charge Injection
- DG401 Dual SPST; Same Pinout as HI5041
- DG403 Dual SPDT; DG190, IH5043, IH5151
- DG405 Dual DPST; DG184, HI5045, IH5145
- TTL, CMOS Compatible
- Single or Split Supply Operation

Benefits

- Low Signal Errors and Distortion
- Reduced Power Supply
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Error
- Simplifies Retrofit
- Simple Interfacing
- Break-Before-Make

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG401, DG403 and DG405 monolithic CMOS analog switches have TTL & CMOS compatible digital inputs, and a voltage reference for logic thresholds.

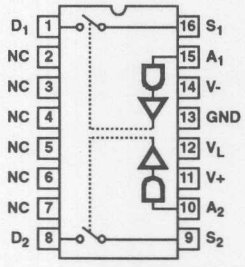
These switches feature low analog ON resistance (< 35Ω) and fast switch time (t_{ON} < 150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401/403/405 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401), two SPDT (DG403) or two DPST (DG405) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permittng a standard layout to be used, choosing the switch function as needed.

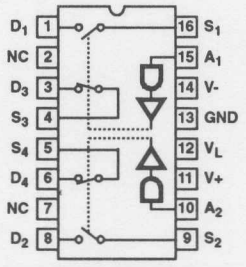
Pinouts Switches Shown for Logic "0" Input

DG401
TOP VIEW



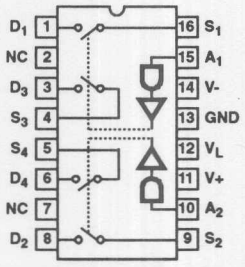
(NC) NO CONNECTION

DG403
TOP VIEW



(NC) NO CONNECTION

DG405
TOP VIEW



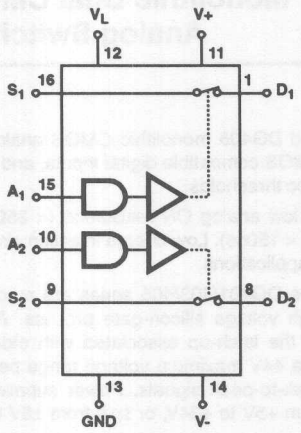
(NC) NO CONNECTION

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

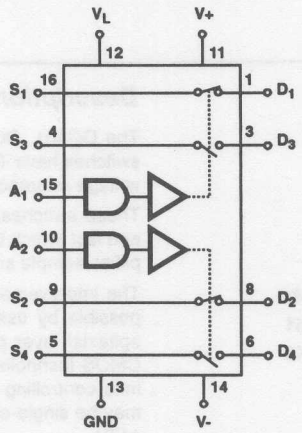
File Number **3284**

Functional Diagrams Switches Shown for Logic "1" Input

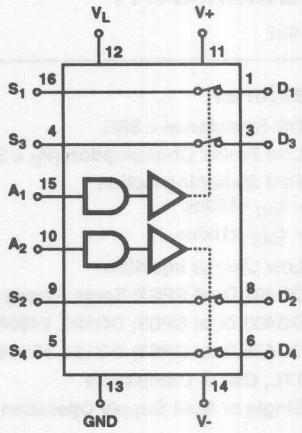
DG401



DG403



DG405



Truth Table

LOGIC	DG401	DG403		DG405
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

HARRIS SEMICONDUCTOR

DG408
DG409

PRELIMINARY

July 1992

Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers

Features

- ON-Resistance 100Ω Maximum (+25°C)
- Low Power Consumption (P_D < 11mW)
- Fast Switching Action
  - t_{TRANS} < 250ns
  - $t_{ON/OFF(EN)}$ < 150ns
- Low Charge Injection
- Upgrade from DG508/DG509
- TTL, CMOS Compatible Logic
- Single or Split Supply Operation

Benefits

- Low Signal Errors and Distortion
- Reduced Power Supply
- Faster Throughput
- Improved Reliability
- Break-Before-Make Switching
- Simplifies Retrofit
- Simple Interfacing

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Description

The DG408 Single 8-Channel and DB409 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular DG508 and DG509 series devices. They each include an array of eight analog switches, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

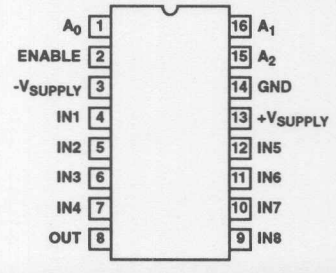
The feature lower signal ON resistance (< 100Ω) and faster switch transition time (t_{TRANS} < 250ns) compared to the DG508A or DG509A. Charge injection has been reduced, simplifying sample and hold applications. The improvements in the DG408 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies.

The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

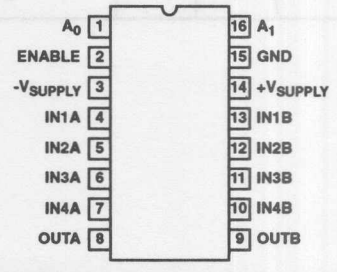
The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Pinouts

DG408
TOP VIEW



DG409
TOP VIEW

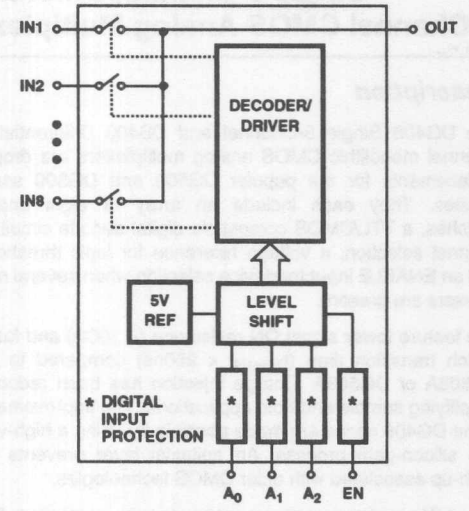


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

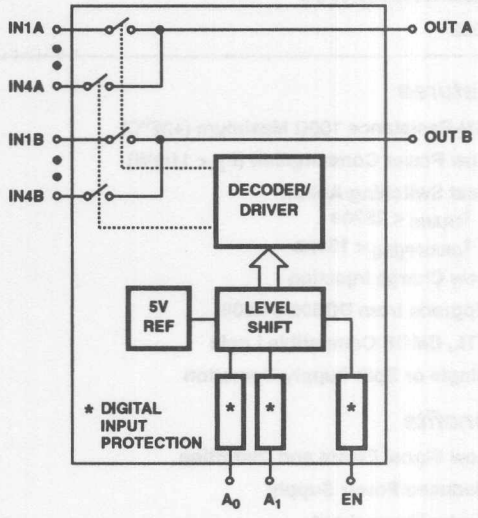
File Number 3280

Functional Block Diagrams

DG408



DG409



Truth Tables

DG408

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG409

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTES:

1. V_{AH} Logic "1" ≥ 2.4V
2. V_{AL} Logic "0" ≤0.8V

HARRIS SEMICONDUCTOR

DG411, DG412 DG413

Monolithic Quad SPST CMOS Analog Switches

PRELIMINARY

July 1992

Features

- ON-Resistance < 35Ω max
- Low Power Consumption (P_D < 35μW)
- Fast Switching Action
  - t_{ON} <175ns
  - t_{OFF} <145ns
- Low Charge Injection
- Upgrade from DG201A/DG202
- TTL, CMOS Compatible
- Single or Split Supply Operation

Benefits

- Low Signal Errors and Distortion
- Reduced Power Supply
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Error
- Simplifies Retrofit
- Simple Interfacing
- DG413 has Two NC, Two NO Switches

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG411 series monolithic CMOS analog switches are drop-in replacements for the popular DG201A and DG202 series devices. They include four independent single pole throw (SPST) analog switches, TTL and CMOS compatible digital inputs and a voltage reference for logic thresholds.

These switches feature lower analog ON resistance (< 35Ω) and faster switch time (t_{ON} < 175ns) compared to the DG201A or DG202. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG411 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The switches in the DG411 and DG412 are identical, differing only in the polarity of the selection logic. Two of the switches in the DG413 (#1 and #4) use the logic of the DG201A/DG411 (i.e. a logic "0" turns the switch ON) and the other two switches use DG202/DG412 positive logic. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting "break-before-make" or "make-before-break" operation with a minimum of external logic.

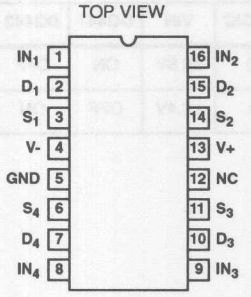
Truth Table

LOGIC	DG411 SWITCH	DG412 SWITCH	DG413 SWITCH 1, 4	DG413 SWITCH 2, 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

Pinout

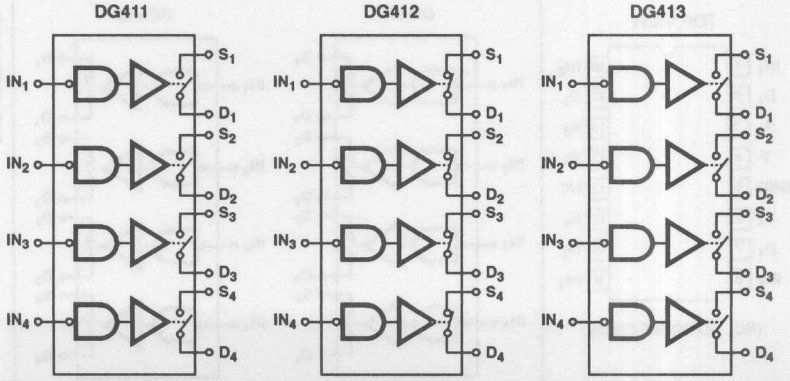
TOP VIEW



(NC) NO CONNECTION

Functional Diagrams

Four SPST Switches per Package Switches Shown for Logic "1" Input



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3281**

HARRIS SEMICONDUCTOR

DG441
DG442

Monolithic Quad SPST CMOS Analog Switches

PRELIMINARY

July 1992

Features

- ON-Resistance 85Ω max
- Low Power Consumption (P_D < 1.6mW)
- Fast Switching Action
  - t_{ON} < 250ns
  - t_{OFF} < 120ns (DG441)
- Low Charge Injection
- Upgrade from DG201A/DG202
- TTL, CMOS Compatible
- Single or Split Supply Operation

Benefits

- Low Signal Errors and Distortion
- Reduced Power Supply
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Error
- Simplifies Retrofit
- Simple Interfacing

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG441 and DG442 monolithic CMOS analog switches are drop-in replacements for the popular DG201A and DG202 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs and a voltage reference for logic thresholds.

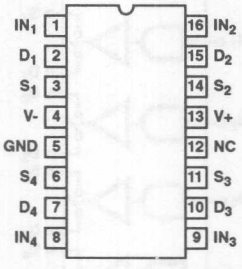
These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} < 250ns) compared to the DG201A and DG202. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG441 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±7V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG441 and DG442 are identical, differing only in the polarity of the selection logic.

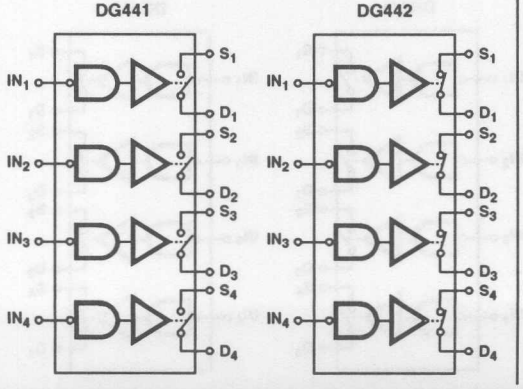
Pinout

TOP VIEW



(NC) NO CONNECTION

Functional Diagrams



Truth Table

LOGIC	VIN	DG441	DG442
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3281**

HARRIS SEMICONDUCTOR

DG458
DG459

PRELIMINARY

July 1992

Single 8 Channel/Differential 4-Channel Fault Protected Analog Multiplexers

Features

- Fault and Overvoltage Protection
- ON-Resistance < 1.8KΩ (+25°C)
- Low Power Consumption (P_D < 6mW)
- Fast Switching Action
  - t_{TRANS} < 500ns
  - $t_{ON/OFF(EN)}$ < 250ns
- Fail Safe with Power Loss (No Latch-Up)
- Upgrade from DG508/DG509
- TTL, CMOS Compatible Logic

Benefits

- Low Signal Errors and Distortion
- Reduced Power Supply
- Faster Throughput
- Improved Reliability
- Break-Before-Make Switching
- Simplifies Retrofit
- Simple Interfacing

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Description

The DG458 Single 8-Channel and DB459 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular DG508 and DG509 series devices. They each include an array of eight analog switches, a series N-channel/P-channel/N-channel fault protection circuit, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

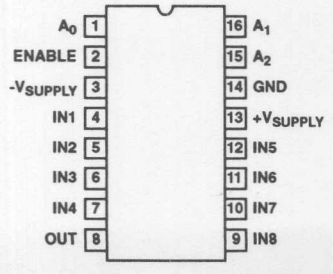
The feature lower signal ON resistance (< 100Ω) and faster switch transition time (t_{TRANS} < 250ns) compared to the DG508A or DG509A. Charge injection has been reduced, simplifying sample and hold applications. The improvements in the DG458 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies.

The 44V maximum voltage range permits controlling 20V peak-to-peak signals, while withstanding continuous overvoltages up to ±35V, providing an open fault circuit.

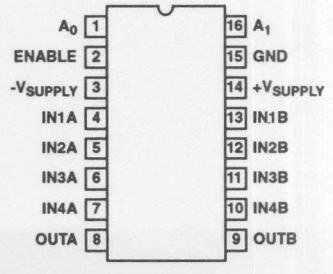
The analog switches are bilateral, break-before-make, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Pinouts

DG458
TOP VIEW



DG459
TOP VIEW

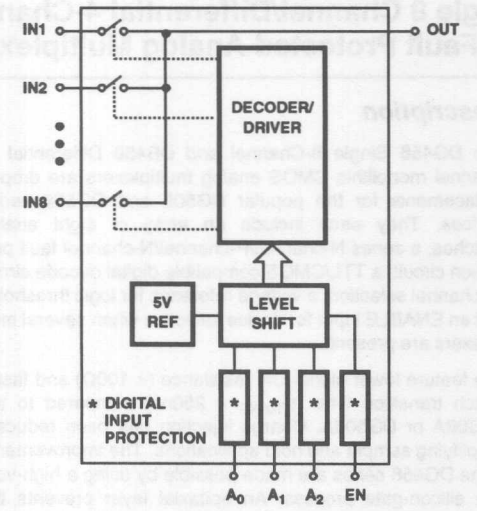


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

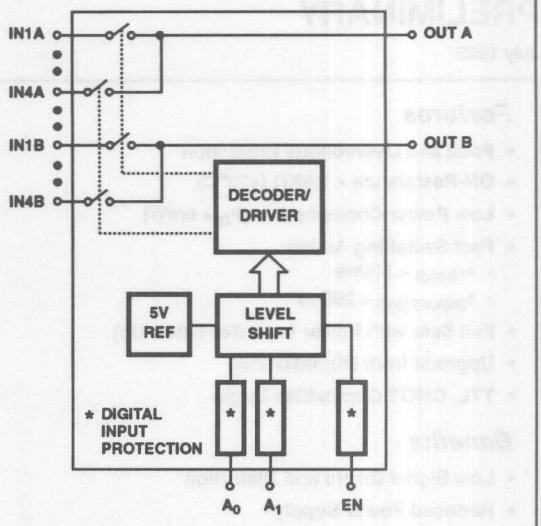
File Number **3280**

Functional Block Diagrams

DG458



DG459



Truth Tables

DG458

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG459

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1A, 1B
0	0	1	2A, 2B
1	0	1	3A, 3B
1	1	1	4A, 4B

NOTES:

1. V_{AH} Logic "1" ≥ 2.4V
2. V_{AL} Logic "0" ≤0.8V

HARRIS SEMICONDUCTOR

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

June 1992

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- 25µs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Improved Second Source for AD574A
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-574A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die feature the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

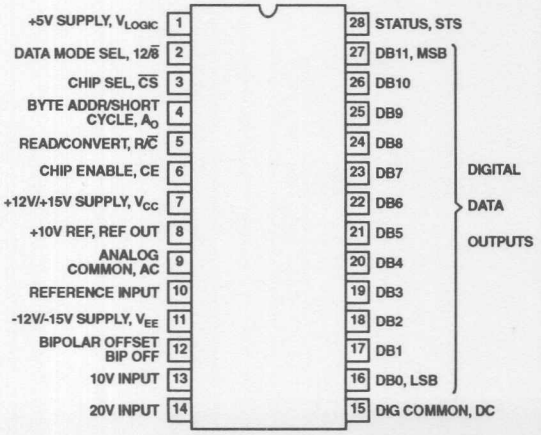
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 ±1µs.

The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. For MIL-STD-883 compliant parts, request the HI-574A/883 data sheet.

Pinout

PLASTIC AND SIDEBRAZE DIP
TOP VIEW



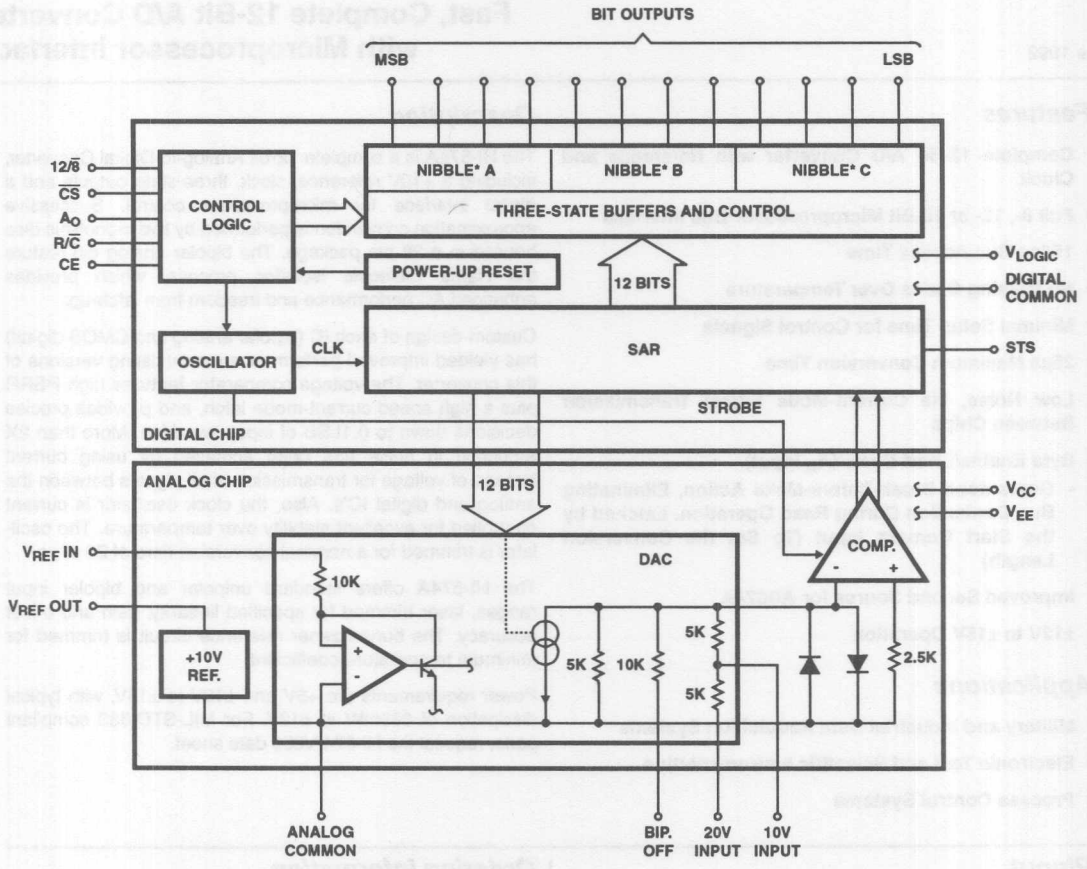
Ordering Information

PART NUMBER	INL	TEMP. RANGE	PACKAGE
HI3-574AJN-5	±1.0LSB	0°C to +75°C	28 Pin Plastic DIP
HI3-574AKN-5	±0.5LSB	0°C to +75°C	28 Pin Plastic DIP
HI1-574AJD-5	±1.0LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-574AKD-5	±0.5LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-574ALD-5	±0.5LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-574ASD-2	±1.0LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-574ATD-2	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-574AUD-2	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-574ASD/883	±1.0LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-574ATD/883	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-574AUD/883	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI4-574ASE/883	±1.0LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-574ATE/883	±0.5LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-574AUE/883	±0.5LSB	-55°C to +125°C	44 Pin Ceramic LCC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3096.1

Functional Block Diagram



* "Nibble" is a 4 bit digital word

Absolute Maximum Ratings

Supply Voltage
- V_{CC} to Digital Common ..... 0V to +16.5V
- V_{EE} to Digital Common ..... 0V to -16.5V
- V_{LOGIC} to Digital Common ..... 0V to +7V
- Analog Common to Digital Common ..... ±1V

Control Inputs
- (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ....-0.5V to V_{LOGIC}+0.5V

Analog Inputs
- (REFIN, BIPOFF, 10VIN) to Analog Common ..... ±16.5V
- 20VIN to Analog Common ..... ±24V

REFOUT .....Indefinite short to Common, momentary short to V_{CC}

Operating Temperature Range
- HI3-574AxN-5, HI1-574AxD-5 .....0°C to +75°C
- HI1-574AxD-2 ..... -55°C to +125°C

Junction Temperature
- HI3-574AxN-5 ..... +150°C
- HI1-574AxD-2, HI1-574AxD-5 ..... +175°C

Storage Temperature Range
- HI3-574AxN-5 .....-40°C < T_A < +85°C
- HI1-574AxD-2, HI1-574AxD-5 .....-65°C < T_A < +150°C

Lead Temperature (Soldering, 10s) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
HI3-574AxN-5	75°C/W	-
HI1-574AxD-2, HI1-574AxD-5	48°C/W	15°C/W

Power Dissipation at 75°C (Note 1)
- HI3-574AxN-5 ..... 1000mW
- HI1-574AxD-2, HI1-574AxD-5 ..... 2083mW

Power Dissipation Derating Factor Above +75°C
- HI3-574AxN-5 ..... 13.3mW/°C
- HI1-574AxD-2, HI1-574AxD-5 ..... 20.8mW/°C

Transistor Count 1117

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC and Transfer Accuracy Specifications

Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS	TEMPERATURE RANGE -5 (0°C to +75°C) HI-574AJ	HI-574AK	HI-574AL	UNITS
Resolution (max)	12	12	12	Bits
Linearity Error				
+25°C (Max)	±1	±1/2	±1/2	LSB
0°C to +75°C (Max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
+25°C (Max resolution for which no missing codes is guaranteed)	±1	±1	±1/2	LSB
+25°C	12	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (max)				
Adjustable to Zero	±2	±1.5	±1	LSB
Bipolar Offset (max)				
V_{IN} = 0V (Adjustable to Zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)	±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)	±0.475	±0.375	±0.20	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)	±0.22	0.12	±0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{MIN} to T_{MAX} (Using internal reference)				
Unipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Bipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Full Scale Calibration	±9 (45)	±2 (10)	±2 (10)	LSB (ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V	±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	±1	LSB

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMPERATURE RANGE -5 (0°C to +75°C) HI-574AJ	HI-574AK	HI-574AL	UNITS
Analog Inputs				
Input Ranges				
Bipolar		-5 to +5		V
		-10 to +10		V
Unipolar		0 to +10		V
		0 to +20		V
Input Impedance				
10V Span		5K, ±25%		Ω
20V Span		10K, ±25%		Ω
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		V
V_{CC}		+11.4 to +16.5		V
V_{EE}		-11.4 to -16.5		V
Operating Current				
I_{LOGIC}		7 Typ, 15 Max		mA
I_{CC} +15V Supply		11 Typ, 15 Max		mA
I_{EE} -15V Supply		21 Typ, 28 Max		mA
Power Dissipation				
±15V, +15V		515 Typ, 720 Max		mW
±12V, +5V		385 Typ		mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max		Volts
Output current (Note 1), available for external loads (External load should not change during conversion).		2.0 Max		mA

NOTE:

1. When supplying an external load (not including the ADC) and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS	TEMPERATURE RANGE -2 (+55°C to +125°C) HI-574AS	HI-574AT	HI-574AU	UNITS
Resolution (max)	12	12	12	Bits
Linearity Error				
+25°C (Max)	±1	±1/2	±1/2	LSB
0°C to +75°C (Max)	±1	±1	±1	LSB
Differential Linearity Error				
+25°C (Max resolution for which no missing codes is guaranteed)	±1	±1	±1/2	LSB
+25°C	12	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (max)				
Adjustable to Zero	±2	±1.5	±1	LSB
Bipolar Offset (max)				
V_{IN} = 0V (Adjustable to Zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)	±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)	±0.75	±0.50	±0.275	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)	±0.50	0.25	±0.125	% of F.S.

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMPERATURE RANGE -2 (+55°C to +125°C) HI-574AS	HI-574AT	HI-574AU	UNITS
Temperature Coefficients				
Guaranteed max change, T_{MIN} to T_{MAX} (Using internal reference)				
Unipolar Offset	±2 (5)	±1 (2.5)	±1 (2.5)	LSB (ppm/°C)
Bipolar Offset	±2 (5)	±2 (5)	±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	±20 (50)	±10 (25)	±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V	±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar		-5 to +5		V
		-10 to +10		V
Unipolar		0 to +10		V
		0 to +20		V
Input Impedance				
10V Span		5kΩ, ±25%		Ω
20V Span		10kΩ, ±25%		Ω
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		V
V_{CC}		+11.4 to +16.5		V
V_{EE}		-11.4 to -16.5		V
Operating Current				
I_{LOGIC}		7 Typ, 15 Max		mA
I_{CC} +15V Supply		11 Typ, 15 Max		mA
I_{EE} -15V Supply		21 Typ, 28 Max		mA
Power Dissipation				
±15V, +15V		515 Typ, 720 Max		mW
±12V, +5V		385 Typ		mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max		Volts
Output current available for external loads (External load should not change during conversion).		2.0 Max		mA

Digital Characteristics (Note 1) All Models, Over Full Temperature Range

PARAMETERS	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, AO, 12/$\overline{8}$) (Note 2)			
Logic "1"	+2.4V		+5.5V
Logic "0"	-0.5V		+0.8V
Current	-5µA	±0.1µA	+5µA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} - 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} - 500µA)	+2.4V		
Leakage (High Z State, DB11-DB0 Only)	-5µA	±0.1µA	+5µA
Capacitance		5pF	

NOTES:

1. See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.
2. Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.

Timing Specifications +25°C, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	-	200	ns
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_0 to CE Setup		0	-	-	ns
t_{HAC}	A_0 Valid During CE High		50	-	-	ns
t_C	Conversion Time	12 Bit Cycle T_{MIN} to T_{MAX}	15	20	25	µs
		8 Bit Cycle T_{MIN} to T_{MAX}	10	13	17	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	-	-	ns
t_{SAR}	A_0 to CE Setup		50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	-	-	ns
t_{HAR}	A_0 Valid After CE Low		50	-	-	ns
t_{HS}	STS Delay After Data Valid		300	-	1200	ns

NOTE:

1. Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs $^1/_2$LSB (1.22mV for 10V span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level $1^1/_2$LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of $\pm^1/_2$LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

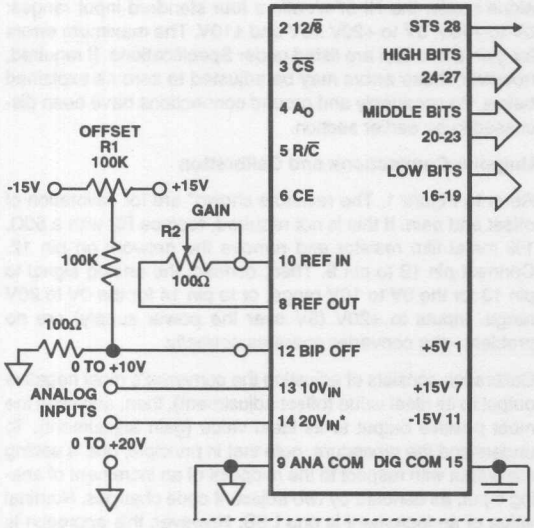
The first transition should occur at a level $^1/_2$LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value $^1/_2$LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value $1^1/_2$LSB below the nominal full scale (9.9963V for 10.000V full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 1 and 2. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10V reference.



*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 1. UNIPOLAR CONNECTIONS

Temperature Coefficients

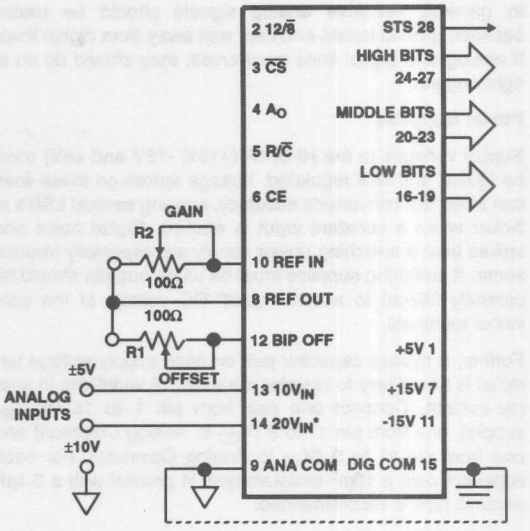
The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10V for a 12-bit ADC.



*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 2. BIPOLAR CONNECTIONS

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm^1/_2$LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-justified Data

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 11 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10µF tantalum type in parallel with a 0.1µF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Common) and 7mADC out of pin 15 (Digital Common. These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-574A analog input will see a nominal load of 5KΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6µs intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5µs after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 1 and 2. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration

Refer to Figure 1. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem - the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of $+^1/_2$LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer RI until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is $1^1/_2$LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 2. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage $^1/_2$LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage $1^1/_2$LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 with a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready-choosing either 12 bits at once or 8 followed by 4 in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 3.

"Stand-Alone Operation"

The simplest control interface calls for a singe control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 4 and 5. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing".

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	300	-	1200	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will

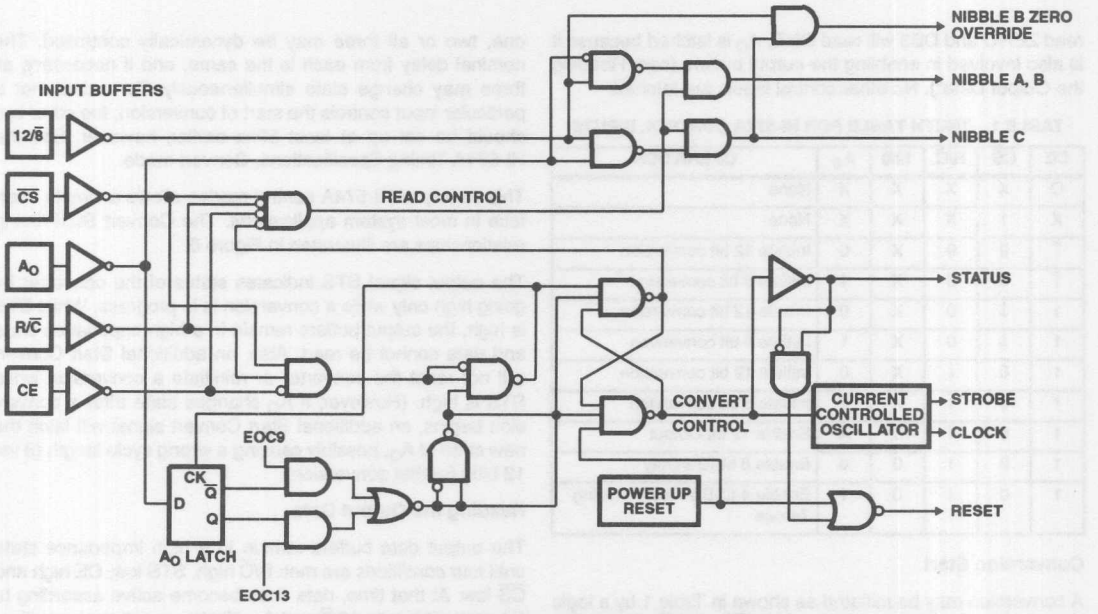


FIGURE 3. HI-574A CONTROL LOGIC

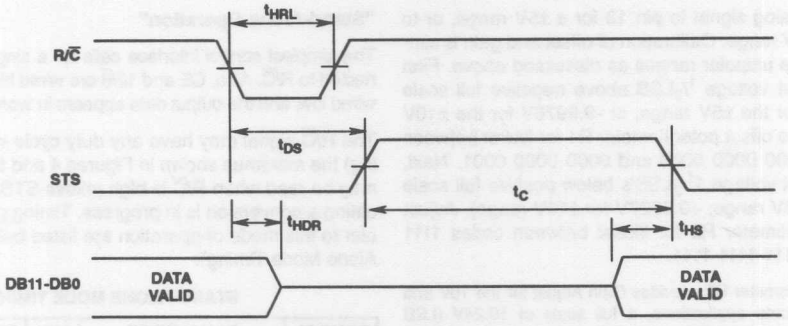


FIGURE 4. LOW PULSE FOR R/C OUTPUTS ENABLED AFTER CONVERSION

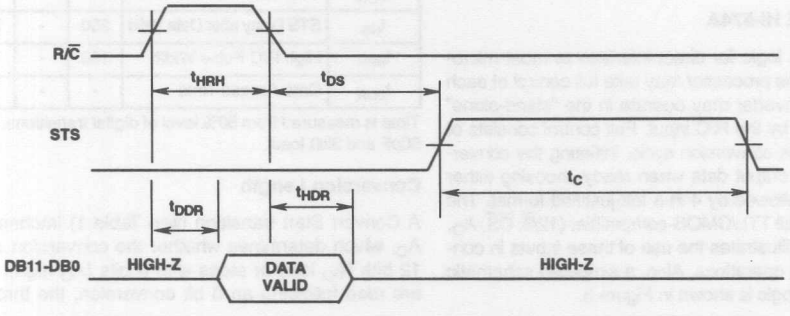


FIGURE 5. HIGH PULSE FOR R/C OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

read ZERO and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HI-574A CONTROL INPUTS

CE	$\overline{CS}$	R/C	12/8	A_0	OPERATION
O	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/C. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier, however. See the HI-574A Timing Specifications, Convert mode.

This variety of HI-574A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 6.

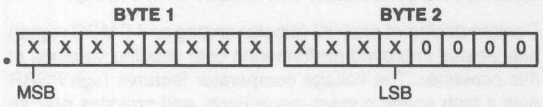
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs. 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/C high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/8 and A_0. Timing constraints are illustrated in Figure 7.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 8. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-574A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 8 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 7.

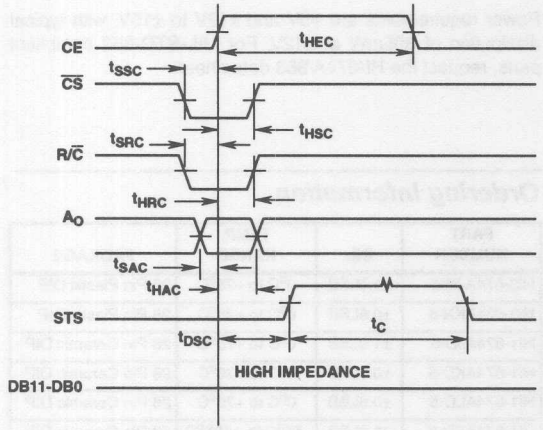


FIGURE 6. CONVERT START TIMING

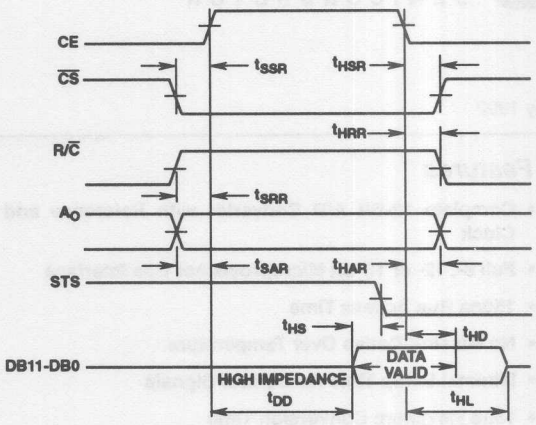


FIGURE 7. READ CYCLE TIMING

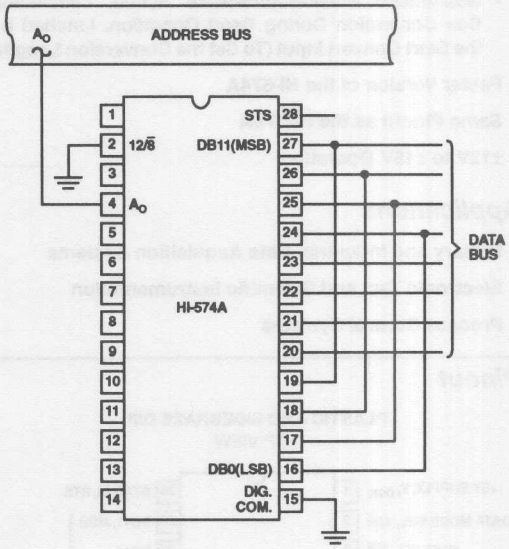


FIGURE 8. INTERFACE TO AN 8 BIT DATA BUS

HARRIS SEMICONDUCTOR

HI-674A

12μs, Complete 12-Bit A/D Converter with Microprocessor Interface

July 1992

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- 15μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A
- Same Pinout as the HI-574A
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-674A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

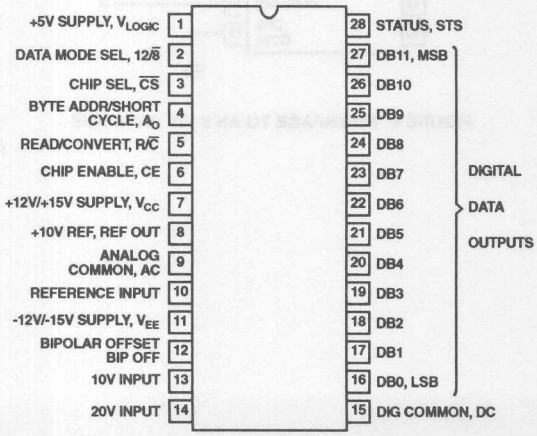
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ±1μs.

The HI-674A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. For MIL-STD-883 compliant parts, request the HI-674A/883 data sheet.

Pinout

PLASTIC AND SIDEBRAZE DIP
TOP VIEW



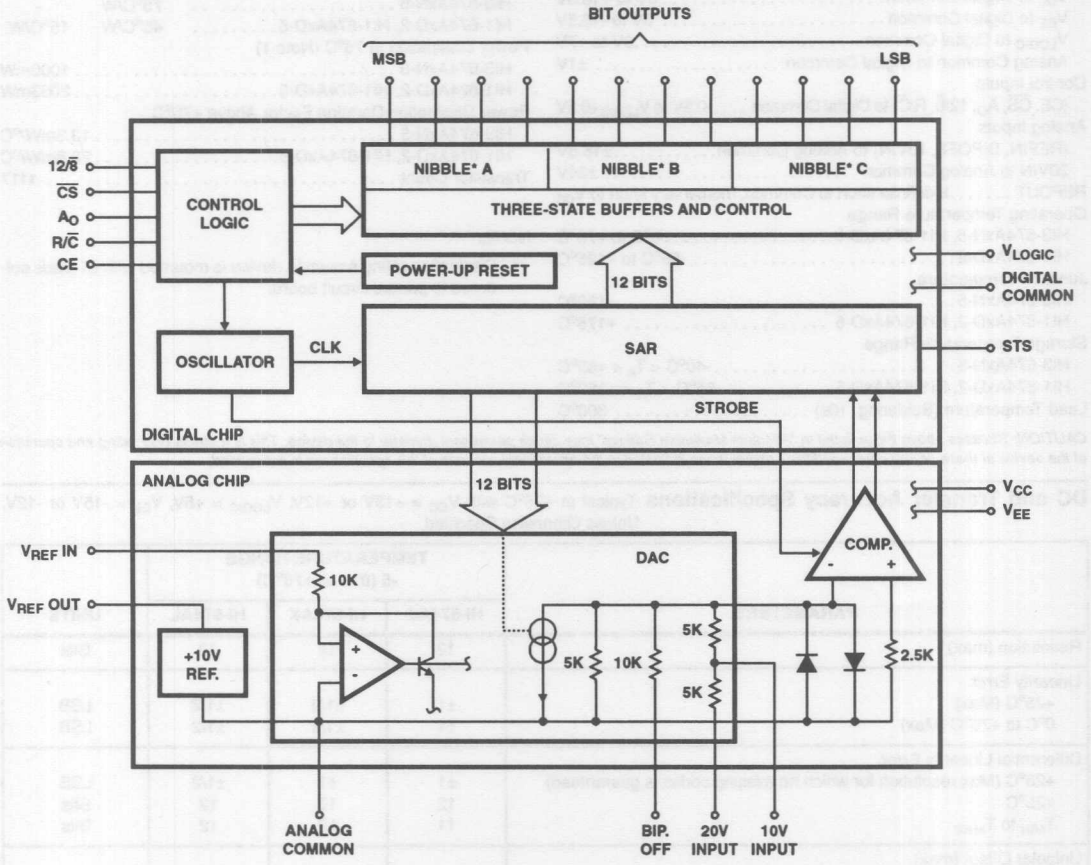
Ordering Information

PART NUMBER	INL	TEMP. RANGE	PACKAGE
HI3-674AJN-5	±1.0LSB	0°C to +75°C	28 Pin Plastic DIP
HI3-674AKN-5	±0.5LSB	0°C to +75°C	28 Pin Plastic DIP
HI1-674AJD-5	±1.0LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-674AKD-5	±0.5LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-674ALD-5	±0.5LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-674ASD-2	±1.0LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674ATD-2	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674AUD-2	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674ASD/883	±1.0LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674ATD/883	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674AUD/883	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI4-674ASE/883	±1.0LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-674ATE/883	±0.5LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-674AUE/883	±0.5LSB	-55°C to +125°C	44 Pin Ceramic LCC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3097.1**

Functional Block Diagram



* "Nibble" is a 4 bit digital word

Absolute Maximum Ratings

Supply Voltage
- V_{CC} to Digital Common ..... 0V to +16.5V
- V_{EE} to Digital Common ..... 0V to -16.5V
- V_{LOGIC} to Digital Common ..... 0V to +7V
- Analog Common to Digital Common ..... ±1V

Control Inputs
- (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ....-0.5V to V_{LOGIC}+0.5V

Analog Inputs
- (REFIN, BIPOFF, 10VIN) to Analog Common ..... ±16.5V
- 20VIN to Analog Common ..... ±24V

REFOUT .....Indefinite short to Common, momentary short to V_{CC}

Operating Temperature Range
- HI3-674AxN-5, HI1-674AxD-5 ..... 0°C to +75°C
- HI1-674AxD-2 ..... -55°C to +125°C

Junction Temperature
- HI3-674AxN-5 ..... +150°C
- HI1-674AxD-2, HI1-674AxD-5 ..... +175°C

Storage Temperature Range
- HI3-674AxN-5 ..... -40°C < T_A < +85°C
- HI1-674AxD-2, HI1-674AxD-5 ..... -65°C < T_A < +150°C

Lead Temperature (Soldering, 10s) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
HI3-674AxN-5	75°C/W	-
HI1-674AxD-2, HI1-674AxD-5	48°C/W	15°C/W

Power Dissipation at 75°C (Note 1)
- HI3-674AxN-5 ..... 1000mW
- HI1-674AxD-2, HI1-674AxD-5 ..... 2083mW

Power Dissipation Derating Factor Above +75°C
- HI3-674AxN-5 ..... 13.3mW/°C
- HI1-674AxD-2, HI1-674AxD-5 ..... 20.8mW/°C

Transistor Count 1117

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC and Transfer Accuracy Specifications

Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS	TEMPERATURE RANGE -5 (0°C to +75°C) HI-674AJ	HI-674AK	HI-674AL	UNITS
Resolution (max)	12	12	12	Bits
Linearity Error				
+25°C (Max)	±1	±1/2	±1/2	LSB
0°C to +75°C (Max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
+25°C (Max resolution for which no missing codes is guaranteed)	±1	±1	±1/2	LSB
+25°C	12	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (max)				
Adjustable to Zero	±2	±1.5	±1	LSB
Bipolar Offset (max)				
V_{IN} = 0V (Adjustable to Zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)	±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)	±0.475	±0.375	±0.20	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)	±0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{MIN} to T_{MAX} (Using internal reference)				
Unipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Bipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Full Scale Calibration	±9 (45)	±2 (10)	±2 (10)	LSB (ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V	±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	±1	LSB

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMPERATURE RANGE -5 (0°C to +75°C)			UNITS
	HI-674AJ	HI-674AK	HI-674AL	
Analog Inputs				
Input Ranges				
Bipolar		-5 to +5 -10 to +10		V V
Unipolar		0 to +10 0 to +20		V V
Input Impedance				
10V Span		5K, ±25%		Ω
20V Span		10K, ±25%		Ω
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		V
V_{CC}		+11.4 to +16.5		V
V_{EE}		-11.4 to -16.5		V
Operating Current				
I_{LOGIC}		7 Typ, 15 Max		mA
I_{CC} +15V Supply		11 Typ, 15 Max		mA
I_{EE} -15V Supply		21 Typ, 28 Max		mA
Power Dissipation				
±15V, +15V		515 Typ, 720 Max		mW
±12V, +5V		385 Typ		mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max		Volts
Output current, available for external loads (External load should not change during conversion).		2.0 Max		mA

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS	TEMPERATURE RANGE -2 (+55°C to +125°C)			UNITS
	HI-674AS	HI-674AT	HI-674AU	
Resolution (max)	12	12	12	Bits
Linearity Error				
+25°C (Max)	±1	±1/2	±1/2	LSB
0°C to +75°C (Max)	±1	±1	±1	LSB
Differential Linearity Error				
+25°C (Max resolution for which no missing codes is guaranteed)	±1	±1	±1/2	LSB
+25°C	12	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (max)				
Adjustable to Zero	±2	±1.5	±1	LSB
Bipolar Offset (max)				
V_{IN} = 0V (Adjustable to Zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)	±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)	±0.75	±0.50	±0.275	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)	±0.50	0.25	±0.125	% of F.S.

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMPERATURE RANGE -2 (+55°C to +125°C) HI-674AS	HI-674AT	HI-674AU	UNITS
Temperature Coefficients				
Guaranteed max change, T_{MIN} to T_{MAX} (Using internal reference)				
Unipolar Offset	±2 (5)	±1 (2.5)	±1 (2.5)	LSB (ppm/°C)
Bipolar Offset	±2 (5)	±2 (5)	±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	±20 (50)	±10 (25)	±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V	±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	-5 to +5			V
	-10 to +10			V
Unipolar	0 to +10			V
	0 to +20			V
Input Impedance				
10V Span	5kΩ, ±25%			Ω
20V Span	10kΩ, ±25%			Ω
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			V
V_{CC}	+11.4 to +16.5			V
V_{EE}	-11.4 to -16.5			V
Operating Current				
I_{LOGIC}	7 Typ, 15 Max			mA
I_{CC} +15V Supply	11 Typ, 15 Max			mA
I_{EE} -15V Supply	21 Typ, 28 Max			mA
Power Dissipation				
±15V, +15V	515 Typ, 720 Max			mW
±12V, +5V	385 Typ			mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}	+10.00 ±0.05 Max			Volts
Output current available for external loads (External load should not change during conversion).	2.0 Max			mA

Digital Characteristics (Note 1) All Models, Over Full Temperature Range

PARAMETERS	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, AO, 12/$\overline{8}$) (Note 2)			
Logic "1"	+2.4V		+5.5V
Logic "0"	-0.5V		+0.8V
Current	-5µA	±0.1µA	+5µA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} - 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} - 500µA)	+2.4V		
Leakage (High Z State, DB11-DB0 Only)	-5µA	±0.1µA	+5µA
Capacitance		5pF	

NOTES:

1. See "HI-674A Timing Specifications" for a detailed listing of digital timing parameters.
2. Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.

Timing Specifications +25°C, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	-	200	ns
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_0 to CE Setup		0	-	-	ns
t_{HAC}	A_0 Valid During CE High		50	-	-	ns
t_C	Conversion Time	12 Bit Cycle T_{MIN} to T_{MAX}	9	12	15	µs
		8 Bit Cycle T_{MIN} to T_{MAX}	6	8	10	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	-	-	ns
t_{SAR}	A_0 to CE Setup		50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	-	-	ns
t_{HAR}	A_0 Valid After CE Low		50	-	-	ns
t_{HS}	STS Delay After Data Valid		25	-	850	ns

NOTE:

1. Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs $^1/_2$LSB (1.22mV for 10V span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level $1^1/_2$LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-674AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of $\pm^1/_2$LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-674AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-674AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-674AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

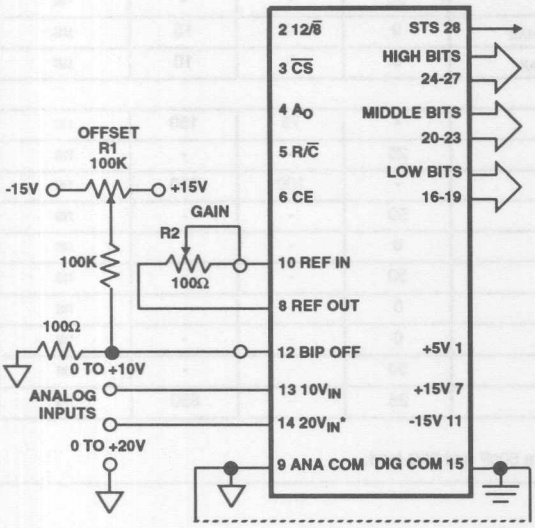
The first transition should occur at a level $^1/_2$LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value $^1/_2$LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value $1^1/_2$LSB below the nominal full scale (9.9963V for 10.000V full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 1 and 2. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10V reference.



*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 1. UNIPOLAR CONNECTIONS

Temperature Coefficients

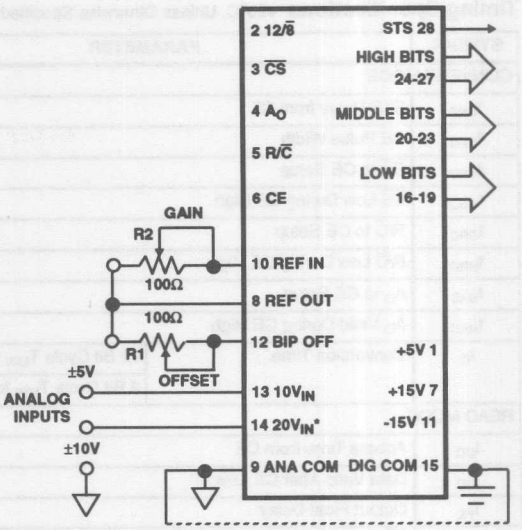
The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection

The standard specifications for the HI-674A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10V for a 12-bit ADC.



*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 2. BIPOLAR CONNECTIONS

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm^1/_2$LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-justified Data

The data format used in the HI-674A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-674A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-674A (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 11 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10µF tantalum type in parallel with a 0.1µF ceramic type is recommended.

Ground Connections

The typical HI-674A ground currents are 6mADC into pin 9 (Analog Common) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-674A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-674A analog input will see a nominal load of 5KΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 950ns intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 1MHz for use with the HI-674A. To check whether the output properties of a signal source are suitable, monitor the 674A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one half microsecond or less. (The comparator decision is made about 850ns after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-674A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-674A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-674A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 1 and 2. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration

Refer to Figure 1. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem - the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of $+^1/_2$LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer RI until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is $1^1/_2$LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 2. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage $^1/_2$LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the +10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage $1^1/_2$LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-674A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready-choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 3.

"Stand-Alone Operation"

The simplest control interface calls for a singe control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 4 and 5. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing".

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	25	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is

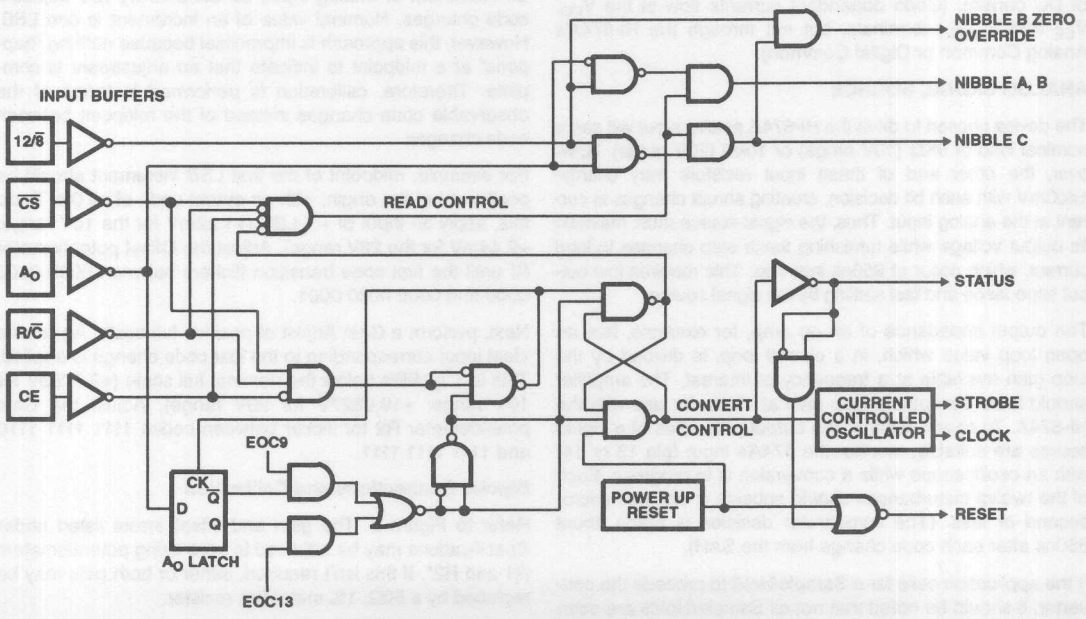


FIGURE 3. HI-674A CONTROL LOGIC

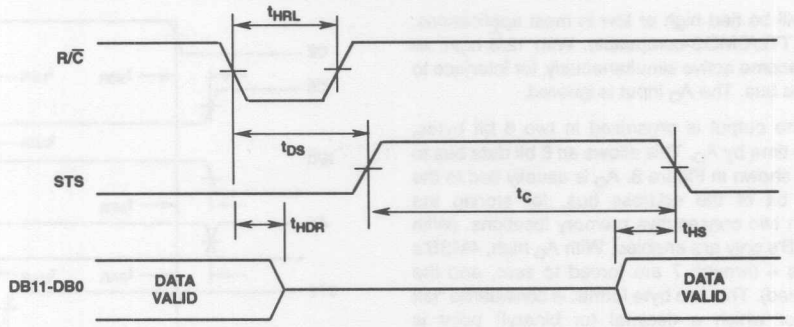


FIGURE 4. LOW PULSE FOR R/C - OUTPUTS ENABLED AFTER CONVERSION

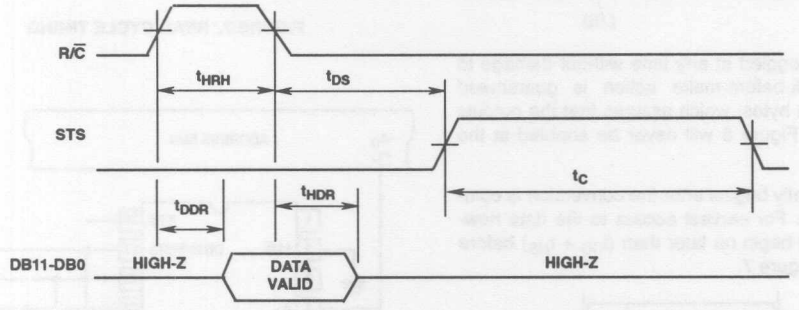


FIGURE 5. HIGH PULSE FOR R/C - OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HI-574A CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
O	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier, however. See the HI-674A Timing Specifications, Convert mode.

This variety of HI-674A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 6.

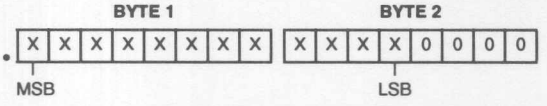
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs. 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 7.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 8. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-674A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 8 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 7.

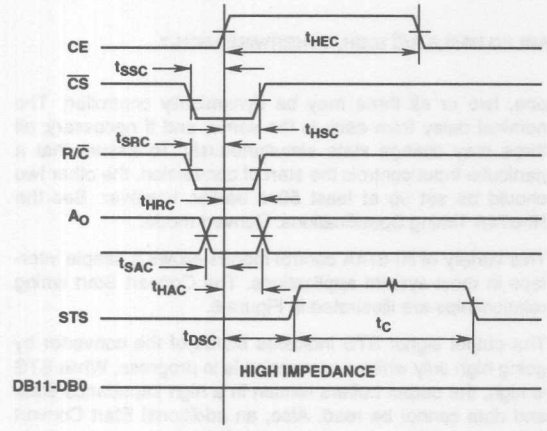


FIGURE 6. CONVERT START TIMING

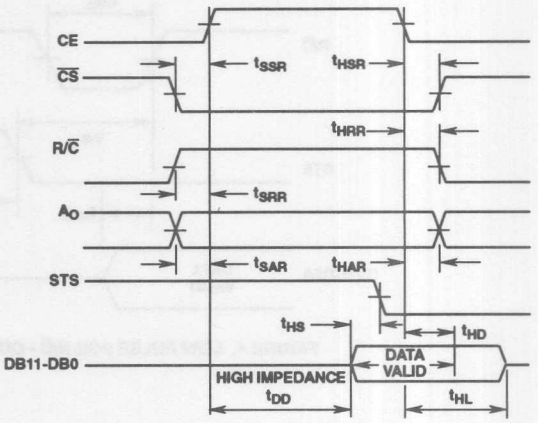


FIGURE 7. READ CYCLE TIMING

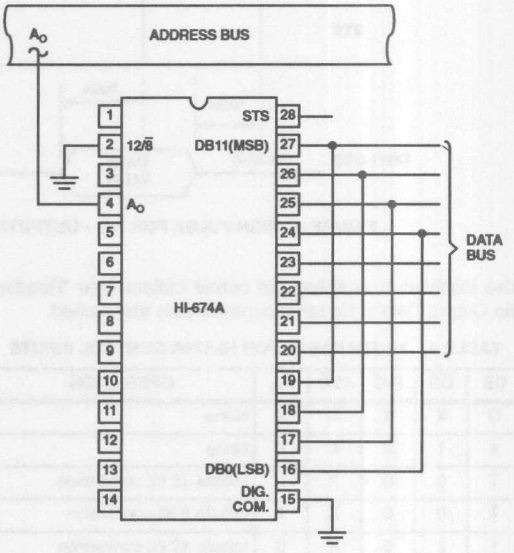


FIGURE 8. INTERFACE TO AN 8 BIT DATA BUS

HARRIS SEMICONDUCTOR

HI-774

8μs, Complete 12-Bit A/D Converter with Microprocessor Interface

July 1992

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Digital Error Correction
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- 9μs Maximum Conversion Time Over Temperature
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A and HI-674A
- Same Pinout as the HI-574A and HI-674A
- ±12V to ±15V Operation

Applications

- Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-774 is a complete 12-bit Analog-to-Digital Converter, including a +10V reference clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up. The digital die features the Smart SAR (SSAR™), which includes a digital error correction circuit.

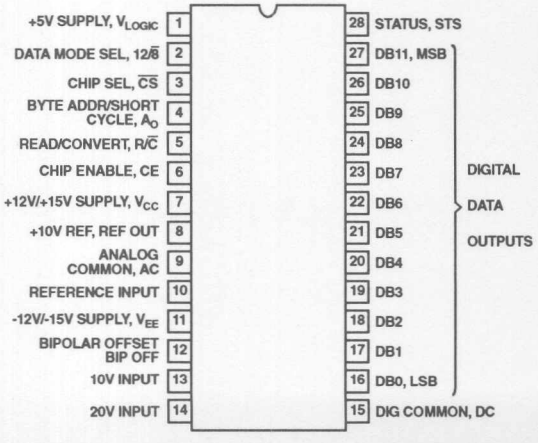
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature.

The HI-774 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 390mW at ±12V. For MIL-STD-883 compliant parts, request the HI-774A/883 data sheet.

Pinout

PLASTIC AND SIDEBRAZE DIP
TOP VIEW



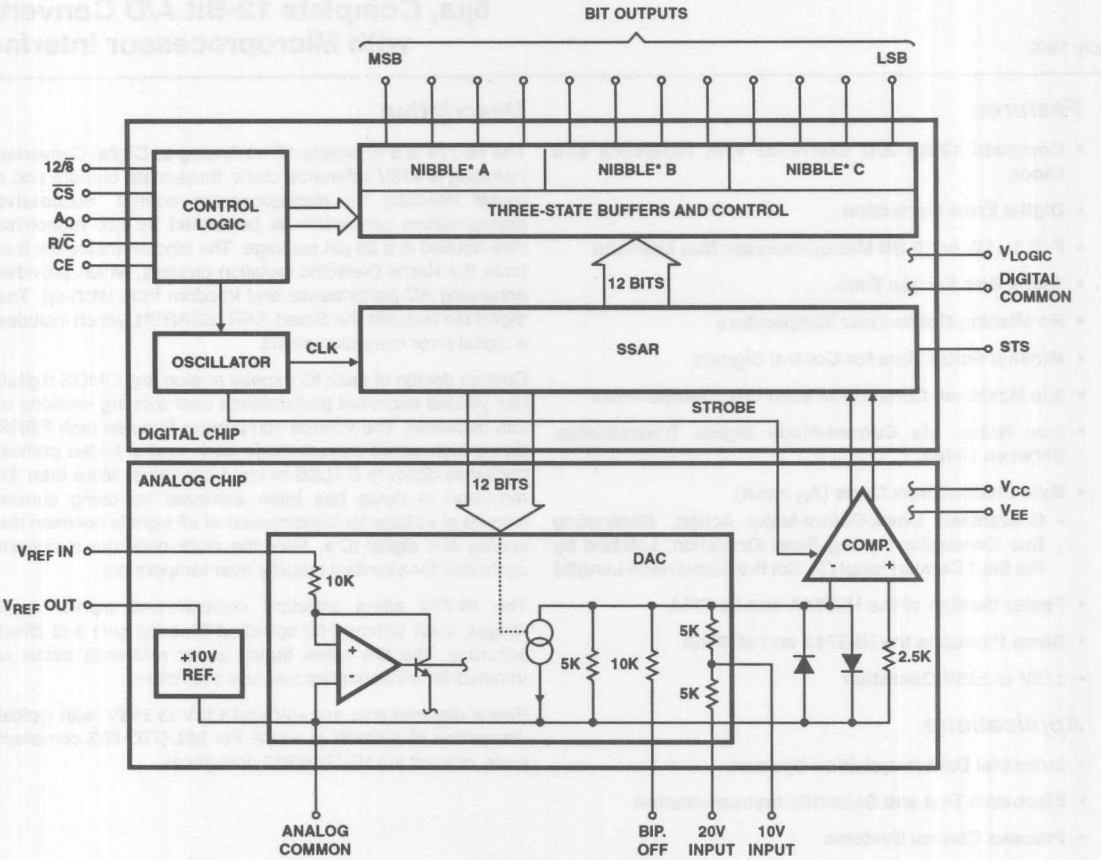
Ordering Information

PART NUMBER	INL	TEMP. RANGE	PACKAGE
HI3-774JN-5	±1.0LSB	0°C to +75°C	28 Pin Plastic DIP
HI3-774KN-5	±0.5LSB	0°C to +75°C	28 Pin Plastic DIP
HI1-774JD-5	±1.0LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-774KD-5	±0.5LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-774LD-5	±0.5LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-774SD-2	±1.0LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774TD-2	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774UD-2	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774S/883	±1.0LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774T/883	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774U/883	±0.5LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI4-774S/883	±1.0LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-774T/883	±0.5LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-774U/883	±0.5LSB	-55°C to +125°C	44 Pin Ceramic LCC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3098.1**

Functional Block Diagram



* "Nibble" is a 4 bit digital word

Absolute Maximum Ratings

Supply Voltage
- V_{CC} to Digital Common ..... 0V to +16.5V
- V_{EE} to Digital Common ..... 0V to -16.5V
- V_{LOGIC} to Digital Common ..... 0V to +7V
- Analog Common to Digital Common ..... ±1V

Control Inputs
- (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ....-0.5V to V_{LOGIC}+0.5V

Analog Inputs
- (REFIN, BIPOFF, $10V_{IN}$) to Analog Common ..... ±16.5V
- $20V_{IN}$ to Analog Common ..... ±24V

REFOUT .....Indefinite short to Common, momentary short to V_{CC}

Operating Temperature Range
- HI3-774xN-5, HI1-774xD-5 ..... 0°C to +75°C
- HI1-774xD-2 ..... -55°C to +125°C

Junction Temperature
- HI3-774xN-5 ..... +150°C
- HI1-774xD-2, HI1-774xD-5 ..... +175°C

Storage Temperature Range
- HI3-774xN-5 ..... -40°C < T_A < +85°C
- HI1-774xD-2, HI1-774xD-5 ..... -65°C < T_A < +150°C

Lead Temperature (Soldering, 10s) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
HI3-774xN-5	75°C/W	-
HI1-774xD-2, HI1-774xD-5	48°C/W	15°C/W

Power Dissipation at 75°C (Note 1)
- HI3-774xN-5 ..... 1000mW
- HI1-774xD-2, HI1-774xD-5 ..... 2083mW

Power Dissipation Derating Factor Above +75°C
- HI3-774xN-5 ..... 13.3mW/°C
- HI1-774xD-2, HI1-774xD-5 ..... 20.8mW/°C

Transistor Count 2117

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC and Transfer Accuracy Specifications

Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS	TEMPERATURE RANGE -5 (0°C to +75°C) HI-774J	HI-774K	HI-774L	UNITS
Resolution (max)	12	12	12	Bits
Linearity Error				
+25°C (Max)	±1	±1/2	±1/2	LSB
0°C to +75°C (Max)	±1	±1/2	±1/2	LSB
Max resolution for which no missing codes is guaranteed				
+25°C	12	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (max)				
Adjustable to Zero	±2	±1.5	±1	LSB
Bipolar Offset (max)				
V_{IN} = 0V (Adjustable to Zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)	±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)	±0.475	±0.375	±0.20	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)	±0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{MIN} to T_{MAX} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
Bipolar Offset	±2	±2	±1	LSB
Full Scale Calibration	±9	±5	±2	LSB
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V	±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	-5 to +5			V
	-10 to +10			V

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMPERATURE RANGE -5 (0°C to +75°C) HI-774J	HI-774K	HI-774L	UNITS
Input Ranges (Continued)				
Unipolar		0 to +10		V
		0 to +20		V
Input Impedance				
10V Span		5K, ±25%		Ω
20V Span		10K, ±25%		Ω
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		V
V_{CC}		+11.4 to +16.5		V
V_{EE}		-11.4 to -16.5		V
Operating Current				
I_{LOGIC}		7 Typ, 15 Max		mA
I_{CC} +15V Supply		11 Typ, 15 Max		mA
I_{EE} -15V Supply		21 Typ, 28 Max		mA
Power Dissipation				
±15V, +15V		515 Typ, 720 Max		mW
±12V, +5V		385 Typ		mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max		Volts
Output current, available for external loads (External load should not change during conversion).		2.0 Max		mA

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS	TEMPERATURE RANGE -2 (+55°C to +125°C) HI-774S	HI-774T	HI-774U	UNITS
Resolution (max)	12	12	12	Bits
Linearity Error				
+25°C (Max)	±1	±1/2	±1/2	LSB
0°C to +75°C (Max)	±1	±1	±1	LSB
Max resolution for which no missing codes is guaranteed				
+25°C	11	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (max)				
Adjustable to Zero	±2	±2	±1	LSB
Bipolar Offset (max)				
V_{IN} = 0V (Adjustable to Zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)	±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)	±0.75	±0.50	±0.275	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)	±0.50	0.25	±0.125	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{MIN} to T_{MAX} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
Bipolar Offset	±2	±2	±1	LSB
Full Scale Calibration	±20	±10	±5	LSB
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V	±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	±1	LSB

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMPERATURE RANGE -2 (+55°C to +125°C) HI-774S	HI-774T	HI-774U	UNITS
Analog Inputs				
Input Ranges				
Bipolar		-5 to +5		V
		-10 to +10		V
Unipolar		0 to +10		V
		0 to +20		V
Input Impedance				
10V Span		5kΩ, ±25%		Ω
20V Span		10kΩ, ±25%		Ω
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		V
V_{CC}		+11.4 to +16.5		V
V_{EE}		-11.4 to -16.5		V
Operating Current				
I_{LOGIC}		7 Typ, 15 Max		mA
I_{CC} +15V Supply		11 Typ, 15 Max		mA
I_{EE} -15V Supply		21 Typ, 28 Max		mA
Power Dissipation				
±15V, +15V		515 Typ, 720 Max		mW
±12V, +5V		385 Typ		mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max		Volts
Output current available for external loads (External load should not change during conversion).		2.0 Max		mA

Digital Specifications All Models, Over Full Temperature Range

PARAMETERS	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 412/$\overline{8}$)			
Logic "1"	+2.4V		+5.5V
Logic "0"	-0.5V		+0.8V
Current		±0.1µA	±5µA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} - 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} - 500µA)	+2.4V		
Logic "1" (I_{SOURCE} - 10µA)	+4.5V		
Leakage (High Z State, DB11-DB0 Only)		±0.1µA	±5µA
Capacitance		5pF	

Timing Specifications +25°C, Unless Otherwise Specified, Into a load with R_L = 3kΩ and C_L = 50pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE	-	100	200	ns
t_{HEC}	CE Pulse Width	50	30	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20	-	ns
t_{SAC}	A_0 to CE Setup	0	0	-	ns
t_{HAC}	A_0 Valid During CE High	50	30	-	ns

Timing Specifications +25°C, Unless Otherwise Specified, Into a load with R_L = 3kΩ and C_L = 50pF **(Continued)**

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
t_C	Conversion Time	12 Bit Cycle T_{MIN} to T_{MAX} (-5)	-	8.0	9	µs
		8 Bit Cycle T_{MIN} to T_{MAX} (-5)	-	6.4	6.8	µs
		12 Bit Cycle T_{MIN} to T_{MAX} (-2)	-	9	11	µs
		8 Bit Cycle T_{MIN} to T_{MAX} (-2)	-	6.8	8.3	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	35	-	ns
t_{HL}	Output Float Delay		-	70	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	0	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	0	-	ns
t_{SAR}	A_0 to CE Setup		50	25	-	ns
t_{HSR}	CS Valid After CE Low		0	0	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	0	-	ns
t_{HAR}	A_0 Valid After CE Low		50	25	-	ns
t_{HS}	STS Delay After Data Valid		-	90	300	ns

NOTE:

1. Time is measured from 50% level of digital transitions, except High Z output conditions which are measured at the 10% or 90% point.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs $^1/_2$LSB (1.22mV for 10V span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level $1^1/_2$LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-774K and L grades are guaranteed for maximum nonlinearity of ±$^1/_2$LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-774J is guaranteed to ±1LSB max error. For this grade, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-774K and L grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-774J grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level $^1/_2$LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value $^1/_2$LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value $1^1/_2$LSB below the nominal full scale (9.9963V for 10.000V full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10V reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection

The standard specifications for the HI-774 assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in

a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10V for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm^1/_2$LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-justified Data

The data format used in the HI-774 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-774

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-774 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSBs to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10µF tantalum type in parallel with a 0.1µF ceramic type is recommended.

Ground Connections

The typical HI-774 ground currents are 6mADC into pin 9 (Analog Common) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) +15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-774's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-774 analog input will see a nominal load of 5KΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a "kick back" glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350ns intervals so an op amp with a low output impedance and fast settling is desirable. Ultimately the input must settle to within the window of Figure 1 at the bit decision points in order to achieve 12 bit accuracy.

The HI-774 differs from the most high-speed successive approximation type ADC's in that it does not require a high performance buffer or sample and hold. With error correction the input can settle while the conversion is underway, but only during the first 4.8µs. The input must be within 10.76% of the final value when the MSB decision is made. This occurs approximately 650ns after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input "kick back" disturbances settle within the window of Figure 1 the device will remain accurate. The combined effect of settling and the "kick back" disturbances must remain in the Figure 1 window.

If the design is being optimized for speed, the input device should have closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of Figure 1.

DIGITAL ERROR CORRECTION

The HI-774 features the smart successive approximation register (SSAR ™) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32LSB window about the final value. The input can move during the first 4.8µs, after which it must remain stable within $\pm^1/_2$LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within $\pm^1/_2$LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 bits). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 bits. This results in a total correction range of +31 to -32 bits. When an 8-bit conversion is performed, the input must settle to within $\pm^1/_2$LSB at 8 bit resolution (which equals ±8 bits at 12-bit resolution).

With the HI-774 a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.8µs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

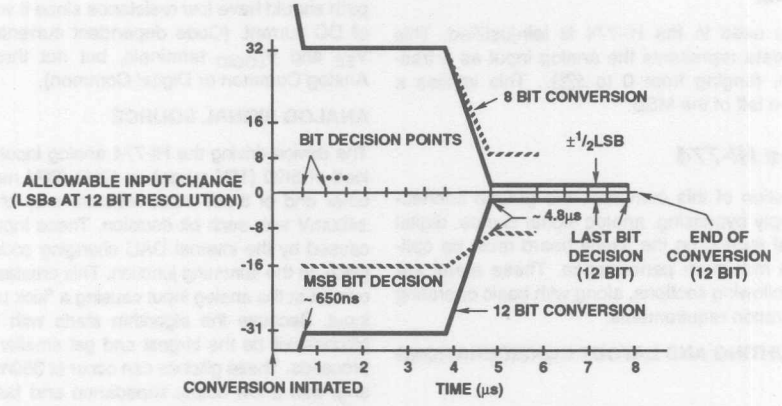


FIGURE 1. HI-774 ERROR CORRECTION WINDOW vs. TIME

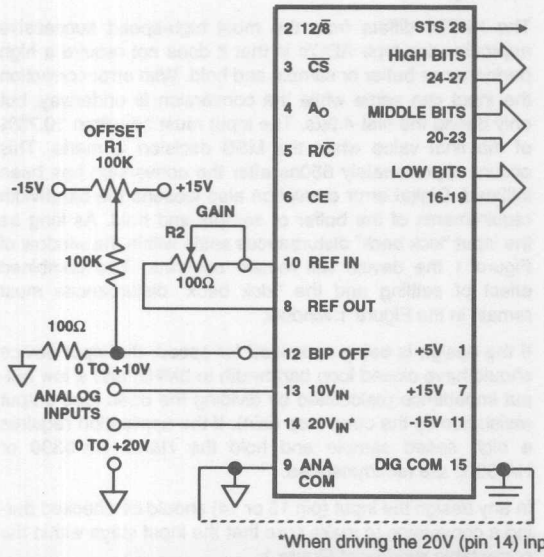
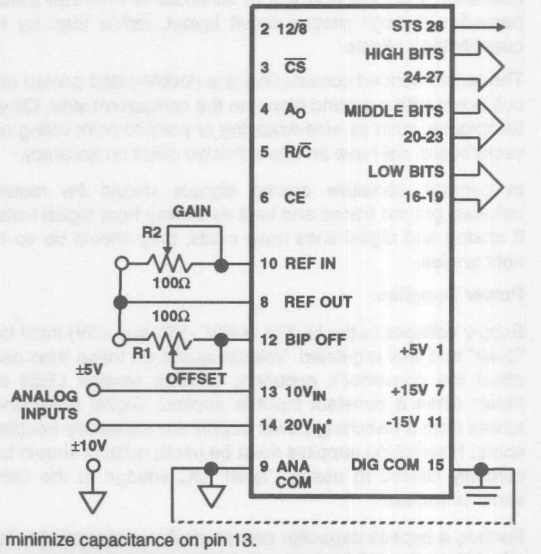


FIGURE 2. UNIPOLAR CONNECTIONS



*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 3. BIPOLAR CONNECTIONS

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-774 is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration

Refer to Figure 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem - the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of $+^1/_2$LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is $1^1/_2$LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage $^1/_2$LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage $1^1/_2$LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

Controlling the HI-774

The HI-774 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready-choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a singe control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing".

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	20	-	-	ns
t_{HS}	STS Delay after Data Valid	-	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

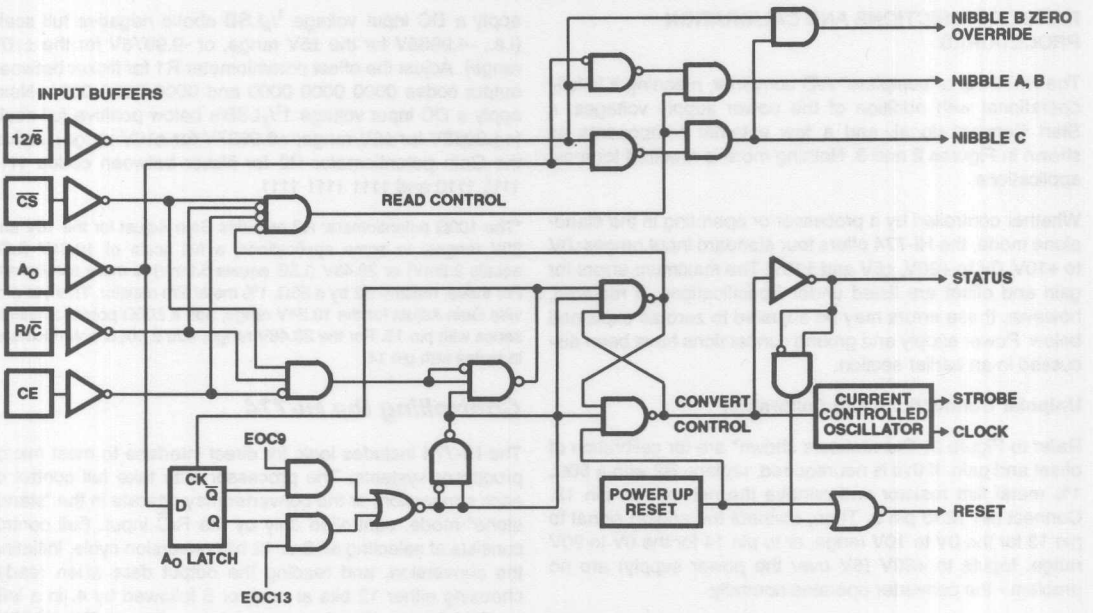


FIGURE 4. HI-774 CONTROL LOGIC

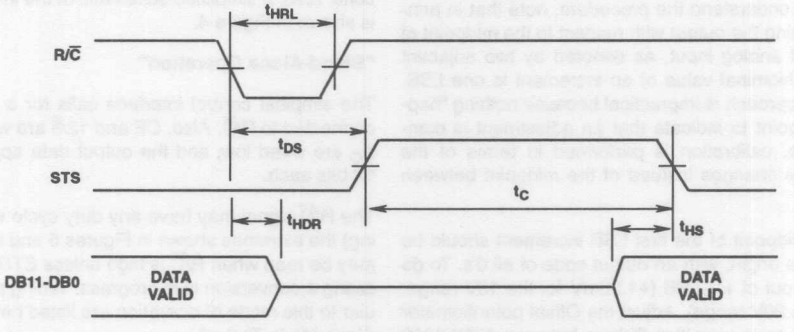


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED AFTER CONVERSION

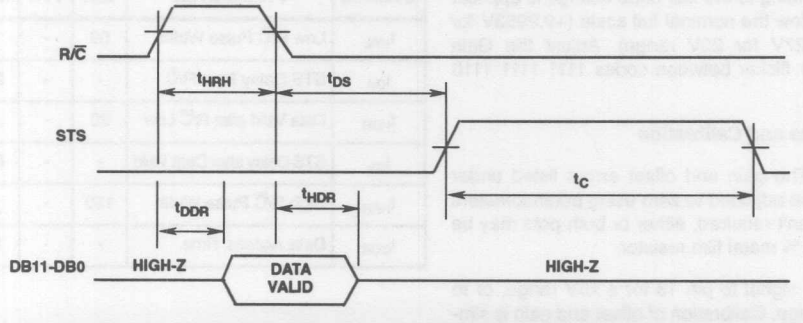


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED WHILE R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the last three LSB's will read ZERO and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HI-774 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
O	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier, however. See the HI-774 Timing Specifications, Convert mode.

This variety of HI-774 control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-774 output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4MSB's are disabled, bits 4 through 7 are forced low, and the 4LSB's are

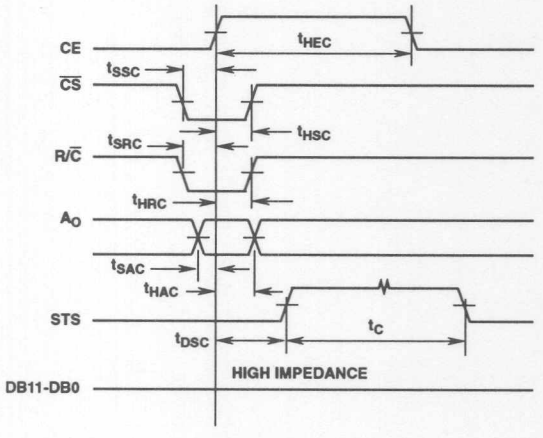


FIGURE 7. CONVERT START TIMING

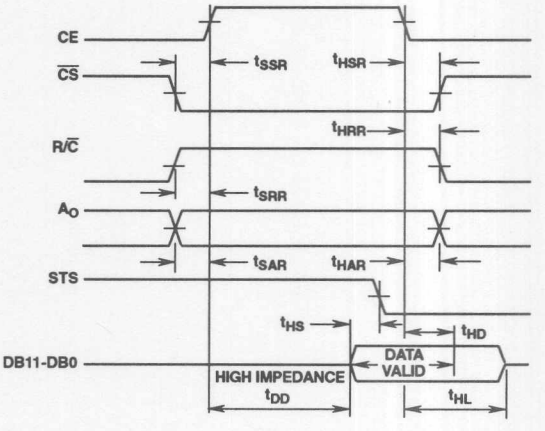
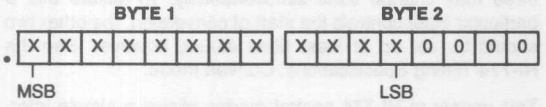


FIGURE 8. READ CYCLE TIMING

See HI-774 Timing Specifications for more information

enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

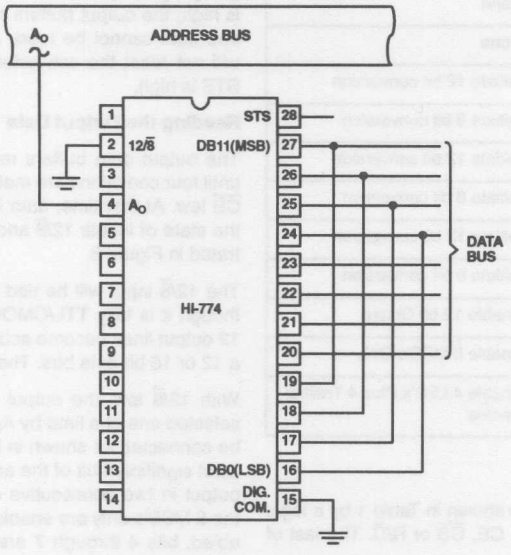


FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

HARRIS SEMICONDUCTOR

HI-5700

July 1992

8-Bit, 20 MSPS Flash A/D Converter

Features

- 20MSPS with No Missing Codes
- 18MHz Full Power Input Bandwidth
- No Missing Codes Over Temperature
- Sample and Hold Not Required
- Single +5V Supply Voltage
- CMOS/TTL
- Overflow Bit
- Improved Replacement for MP7684

Applications

- Video Digitizing
- Radar Systems
- Medical Imaging
- Communication Systems
- High Speed Data Acquisition Systems

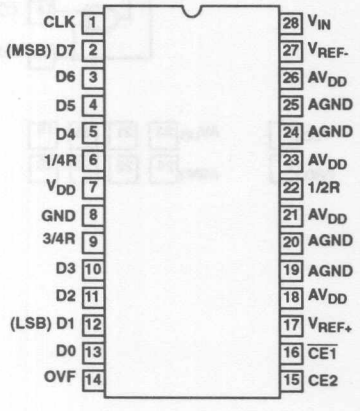
Description

The HI-5700 is a monolithic, 8 bit, CMOS Flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 20MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5700 delivers ±0.5LSB differential nonlinearity while consuming only 725mW (typical) at 20MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 9 bit resolution.

The HI-5700 is available in Commercial and Industrial temperature ranges and is supplied in 28 pin Plastic DIP and SOIC packages.

Pinout

28 PLASTIC DIP AND SOIC
TOP VIEW



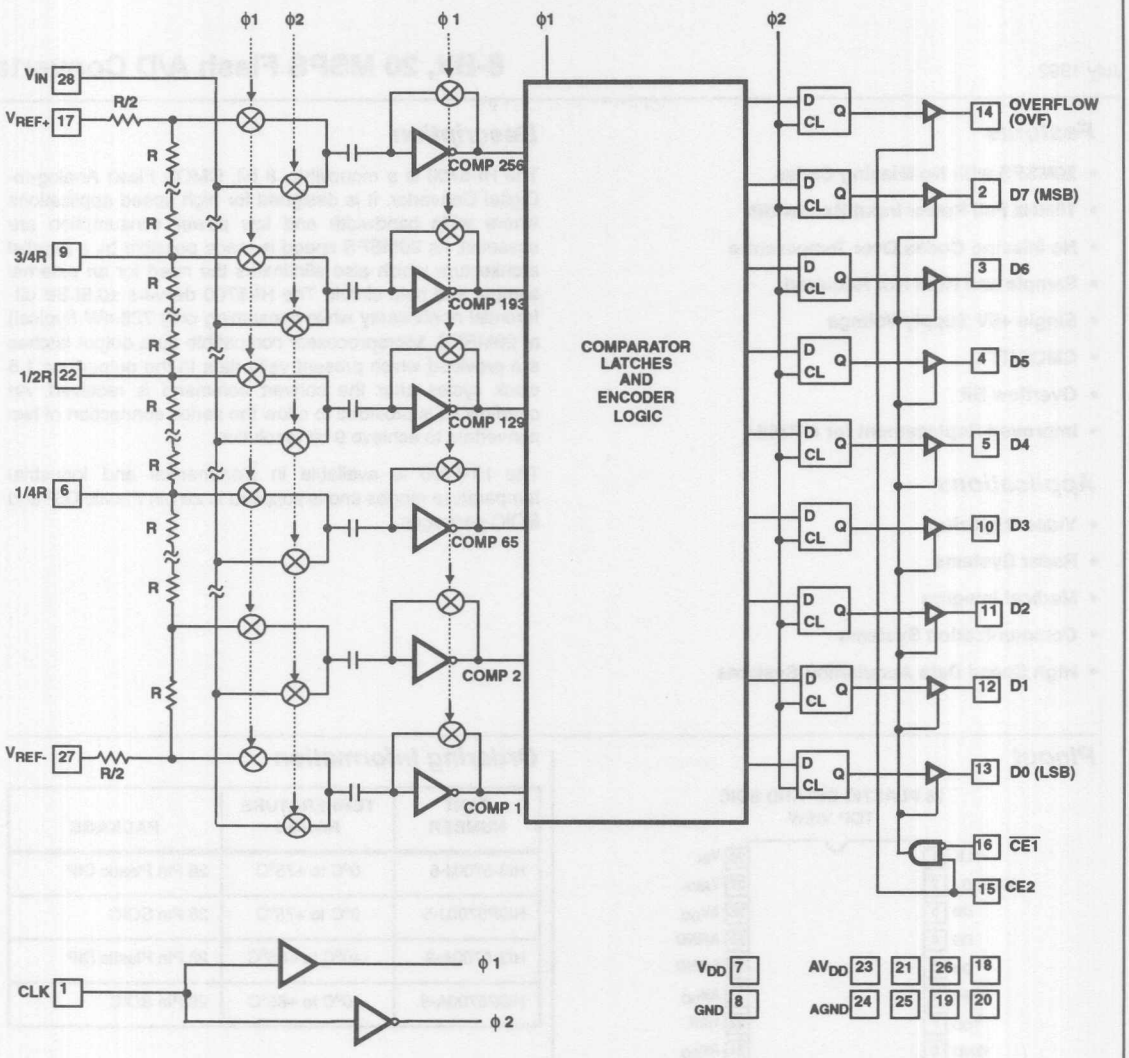
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-5700J-5	0°C to +75°C	28 Pin Plastic DIP
HI9P5700J-5	0°C to +75°C	28 Pin SOIC
HI3-5700A-9	-40°C to +85°C	28 Pin Plastic DIP
HI9P5700A-9	-40°C to +85°C	28 Pin SOIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3174.2**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to GND ..... (GND - 0.5) < V_{DD} < +7.0V
Analog and Reference Input Pins.... (V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)
Digital I/O Pins ..... (GND - 0.5) < $V_{I/O}$ < (V_{DD} +0.5V)
Operating Temperature Range
HI3-5700J-5, HI9P5700J-5.....0°C to +75°C
HI3-5700A-9, HI9P5700A-9 ..... -40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
HI3-5700J-5, HI3-5700A-9	50°C/W	20°C/W
HI9P5700J-5, HI9P5700A-9	71°C/W	22°C/W

Power Dissipation at +75°C (Note 1)
HI3-5700J-5, HI3-5700A-9 ..... 1500mW
HI9P5700J-5, HI9P5700A-9 ..... 1100mW
Power Dissipation Derating Factor Above +75°C
HI3-5700J-5, HI3-5700A-5 ..... 20mW/°C
HI9P5700J-5, HI9P5700A-9 ..... 14mW/°C

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications

$AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency @ 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

PARAMETER	TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	(NOTE 2) 0°C to +75°C -40°C to +85°C MIN	(NOTE 2) 0°C to +75°C -40°C to +85°C MAX	UNITS
ACCURACY							
Resolution		8			8		Bits
Integral Linearity Error (INL) (Best Fit Method)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±0.9 ±1.0	±2.0 ±2.25		±2.25 ±3.25	LSB LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±0.4 ±0.5	±0.9 ±0.9		±1.0 ±1.0	LSB LSB
Offset Error (VOS)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±5.0 ±5.0	±8.0 ±8.0		±9.5 ±9.5	LSB LSB
Full Scale Error (FSE)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±0.5 ±0.6	±4.5 ±4.5		±8.0 ±8.0	LSB LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	20	25		20		MSPS
Minimum Conversion Rate	No Missing Codes (Note 2)			0.125		0.125	MSPS
Full Power Input Bandwidth	F_S = 20MHz		18				MHz
Signal to Noise Ratio (SNR) = RMS Signal / RMS Noise	F_S = 15MHz, f_{IN} = 100kHz F_S = 15MHz, f_{IN} = 3.58MHz F_S = 15MHz, f_{IN} = 4.43MHz F_S = 20MHz, f_{IN} = 100kHz F_S = 20MHz, f_{IN} = 3.58MHz F_S = 20MHz, f_{IN} = 4.43MHz		46.5 44.0 43.4 45.9 42.0 41.6				dB dB dB dB dB dB
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion	F_S = 15MHz, f_{IN} = 100kHz F_S = 15MHz, f_{IN} = 3.58MHz F_S = 15MHz, f_{IN} = 4.43MHz F_S = 20MHz, f_{IN} = 100kHz F_S = 20MHz, f_{IN} = 3.58MHz F_S = 20MHz, f_{IN} = 4.43MHz		43.4 34.3 32.3 42.3 35.2 32.8				dB dB dB dB dB dB

Electrical Specifications $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency @ 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	(NOTE 2) 0°C to +75°C -40°C to +85°C MIN	(NOTE 2) 0°C to +75°C -40°C to +85°C MAX	UNITS
Total Harmonic Distortion	F_S = 15MHz, f_{IN} = 100kHz		-46.9				dBc
	F_S = 15MHz, f_{IN} = 3.58MHz		-34.8				dBc
	F_S = 15MHz, f_{IN} = 4.43MHz		-32.8				dBc
	F_S = 20MHz, f_{IN} = 100kHz		-46.6				dBc
	F_S = 20MHz, f_{IN} = 3.58MHz		-36.6				dBc
	F_S = 20MHz, f_{IN} = 4.43MHz		-33.5				dBc
Differential Gain	F_S = 14MHz, f_{IN} = 3.58MHz		3.5				%
Differential Phase Error	F_S = 14MHz, f_{IN} = 3.58MHz		0.9				Degree
ANALOG INPUT							
Analog Input Resistance, R_{IN}	V_{IN} = 4V	4	10				MΩ
Analog Input Capacitance, C_{IN}	V_{IN} = 0V		60				pF
Analog Input Bias Current, IB	V_{IN} = 0V, 4V		±0.01	±1.0		±1.0	µA
REFERENCE INPUT							
Total Reference Resistance, R_L		250	330		235		Ω
Reference Resistance Tempco, T_C			+0.31				Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0			2.0		V
Input Logic Low Voltage, V_{IL}				0.8		0.8	V
Input Logic High Current, I_{IH}	V_{IN} = 5V			1.0		1.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V			1.0		1.0	µA
Input Capacitance, C_{IN}			7				pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2			3.2		mA
Output Logic Source Current, I_{OH}	V_O = 4.5V	-3.2			-3.2		mA
Output Leakage, I_{OZ}	CE2 = 0V, V_O = 0V, 5V			±1.0		±1.0	µA
Output Capacitance, C_{OUT}	CE2 = 0V		5.0				pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}			6				ns
Aperture Jitter, t_{AJ}			30				ps
Data Output Enable Time, t_{EN}			18	25		30	ns
Data Output Disable Time, t_{DIS}			15	20		25	ns
Data Output Delay, t_{OD}			20	25		30	ns
Data Output Hold, t_H		10	20		5		ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔVOS	V_{DD} = 5V ±10%		±0.1	±2.75		±5.0	LSB
Gain Error PSRR, ΔFSE	V_{DD} = 5V±10%		±0.1	±2.75		±5.0	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	F_S = 20MHz		145	180		190	mA

NOTE:

2. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

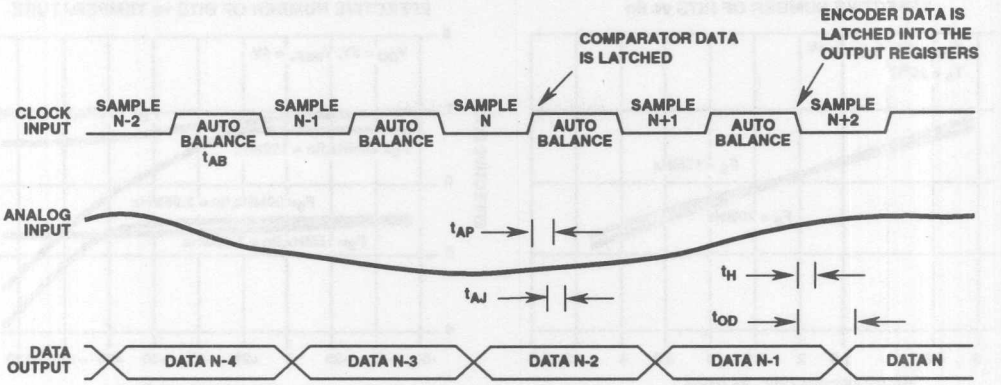


FIGURE 1. INPUT-TO-OUTPUT TIMING

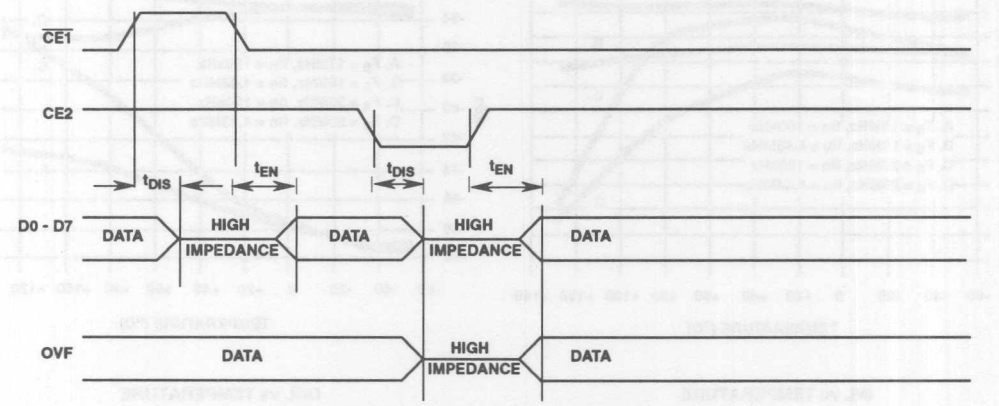
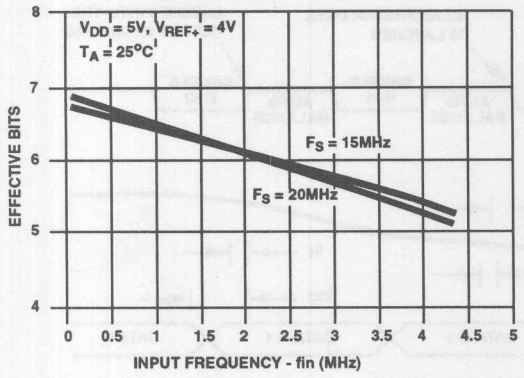


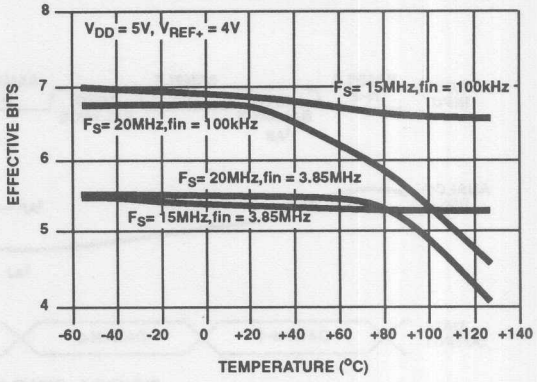
FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

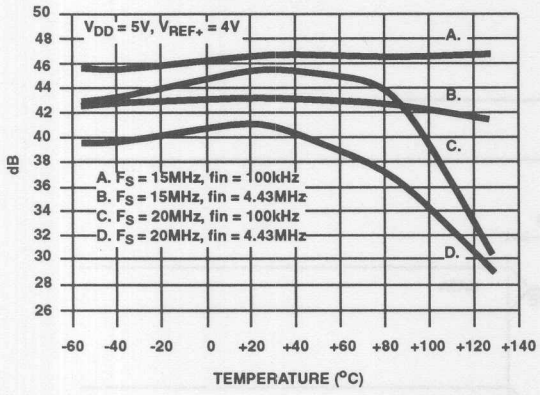
EFFECTIVE NUMBER OF BITS vs fin



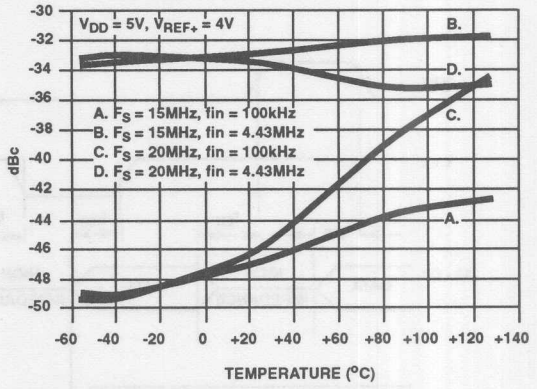
EFFECTIVE NUMBER OF BITS vs TEMPERATURE



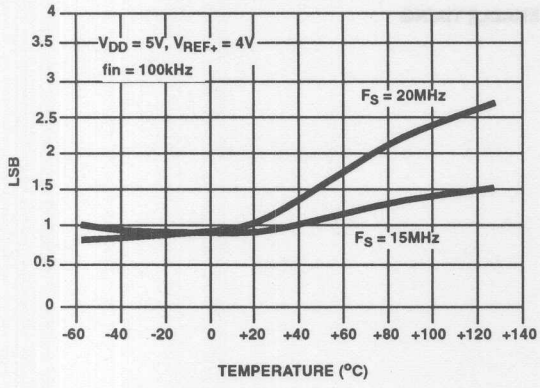
SNR vs TEMPERATURE



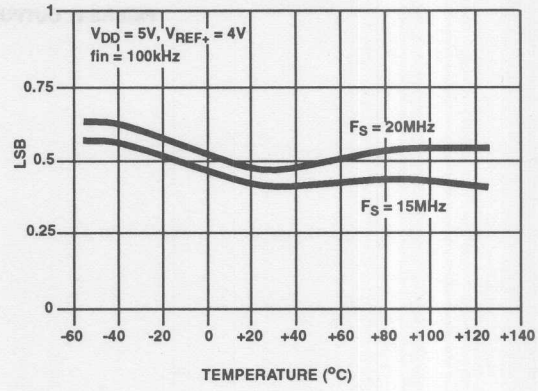
TOTAL HARMONIC DISTORTION vs TEMPERATURE



INL vs TEMPERATURE

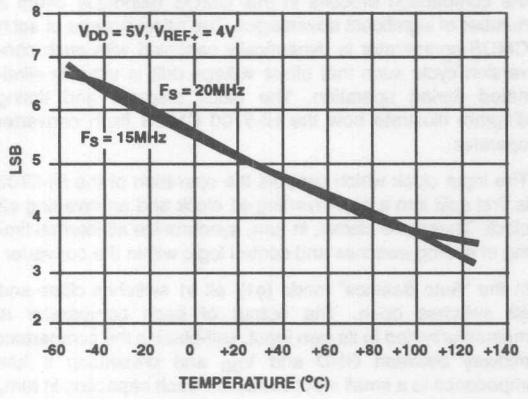


DNL vs TEMPERATURE

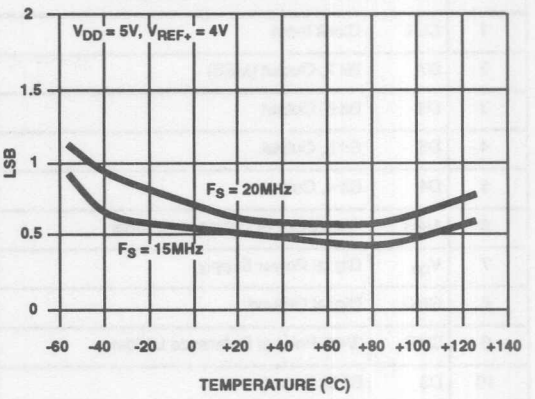


Typical Performance Curves (Continued)

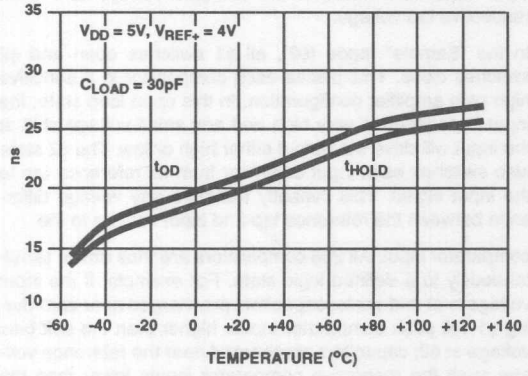
OFFSET VOLTAGE vs. TEMPERATURE



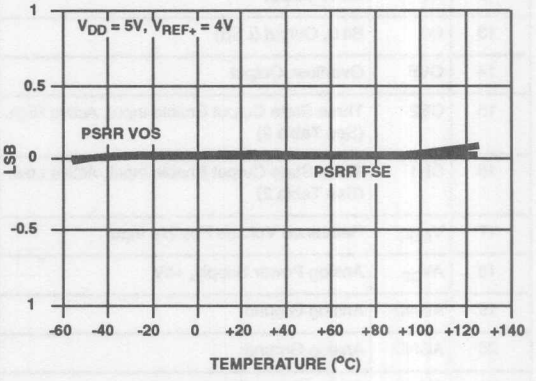
FULL SCALE ERROR vs TEMPERATURE



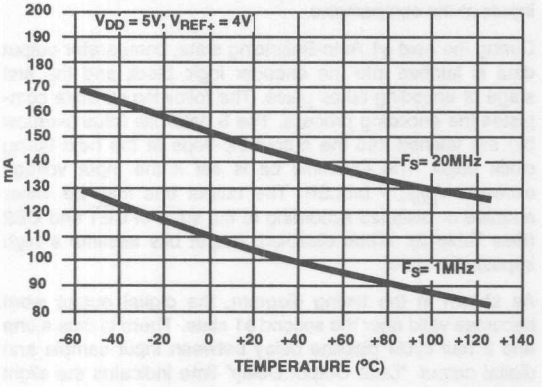
OUTPUT DELAY vs TEMPERATURE



POWER SUPPLY REJECTION vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs CLOCK & DUTY CYCLE

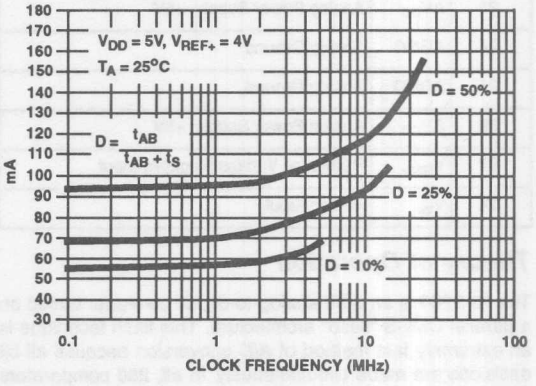


TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	CLK	Clock Input
2	D7	Bit 7, Output (MSB)
3	D6	Bit 6, Output
4	D5	Bit 5, Output
5	D4	Bit 4, Output
6	1/4R	1/4th Point of Reference Ladder
7	V_{DD}	Digital Power Supply
8	GND	Digital Ground
9	3/4R	3/4th Point of Reference Ladder
10	D3	Bit 3, Output
11	D2	Bit 2, Output
12	D1	Bit 1, Output
13	D0	Bit 0, Output (LSB)
14	OVF	Overflow, Output
15	CE2	Three State Output Enable Input, Active High. (See Table 2)
16	$\overline{CE1}$	Three State Output Enable Input, Active Low. (See Table 2)
17	V_{REF+}	Reference Voltage Positive Input
18	AV_{DD}	Analog Power Supply, +5V
19	AGND	Analog Ground
20	AGND	Analog Ground
21	AV_{DD}	Analog Power Supply, +5V
22	1/2R	1/2 Point of Reference Ladder
23	AV_{DD}	Analog Power Supply, +5V
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Analog Power Supply, +5V
27	V_{REF-}	Reference Voltage Negative Input
28	V_{IN}	Analog Input

Theory of Operation

The HI-5700 is an 8 bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 256 comparators are used in the HI-5700: (2^8-1) comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5700 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5700 CMOS flash converter operates.

The input clock which controls the operation of the HI-5700 is first split into a non-inverting ϕ1 clock and an inverting ϕ2 clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter

In the "Auto Balance" mode (ϕ1), all ϕ1 switches close and ϕ2 switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between GND and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 256 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode (ϕ2), all ϕ1 switches open and ϕ2 switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The ϕ2 state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the

comparator input. All 256 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during ϕ1 will push comparator inputs higher than the self bias voltage at ϕ2; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next ϕ1 Auto-Balancing state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following ϕ2 state completes the encoding process. The 8 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds V_{REF+} - 0.5LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second ϕ1 state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the ϕ1 state.

Applications Information

Voltage Reference

The reference voltage is applied across the resistor ladder between V_{REF+} and V_{REF-}. In most applications, V_{REF-} is simply tied to analog ground such that the reference source drives V_{REF+}. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235Ω over temperature.

The HI-5700 is specified for a reference voltage of 4.0 volts, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0 volt reference operation, the converter encodes the analog input into a binary output in LSB increments of (V_{REF+} - V_{REF-})/256, or 15.6mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2.5 volts. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01µF and 10µF) capacitors near the package pin are recommended. It is not necessary to decouple the 1/4R, 1/2R, and 3/4R tap point pins for most applications.

It is possible to elevate V_{REF-} from ground if necessary. In this case, the V_{REF-} pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5700 provides a standard high speed interface to external CMOS and TTL logic families. Two chip enable inputs control the three-state outputs of output bits D0 through D7 and the Overflow (OVF) bit. As indicated in the Truth Table, all output bits are high impedance when CE2 is low, and output bits D0 through D7 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local group disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the "Theory of Operation" section. The Auto Balance ϕ1 half cycle of the clock may be reduced to approximately 20ns; the Sample ϕ2 half cycle may be varied from a minimum of 25ns to a maximum of 5µs.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feedthrough in the capacitor array. It varies with the amplitude of the analog input and the converter's sampling rate.

The signal source must absorb these transients prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HFA-0005, HA-5004, HA-5002, and HA-5003.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +0.5LSB are converted to all zeroes; input voltages of V_{REF+} -0.5LSB to V_{DD} +0.5V are converted to all ones with the Overflow bit set.

Full Scale Offset Error Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and reference tap point trims. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

Offset correction can be done in the preamp driving the converter by introducing a DC component to the input signal. An alternate method is to adjust V_{REF-} to produce the desired offset. It is adjusted such that the 0 to 1 code transition occurs at 0.5LSB.

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the V_{REF+} voltage. The reference voltage is the ideal location.

Quarter Point Adjustment

The reference tap points are brought out for linearity adjustment or creating a nonlinear transfer function if desired. It is not necessary to decouple the 1/4R, 1/2R, and 3/4R tap points in most applications.

Power Supplies

The HI-5700 operates nominally from 5 volt supplies but will work from 3 volts to 6 volts. Power to the device is split such that analog and digital circuits within the HI-5700 are powered separately. The analog supply should be well regulated and "clean" from significant noise, especially high frequency noise. The digital supply should match the analog supply within about 0.5 volts and should be referenced externally to the analog supply at a single point. Analog and digital grounds should not be separated by more that 0.5 volts. It is recommended that power supply decoupling capacitors be placed as close to the supply pins as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors is recommended for this purpose as shown in the test circuit.

Reducing Power Consumption

Power dissipation in the HI-5700 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by decreasing the Auto-Balance (ϕ1) portion of the clock duty cycle. This relationship is illustrated in the performance curves.

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D7	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X's = Don't Care.

TABLE 3. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* V_{REF+} = 4.0V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB								LSB
			OVF	D7	D6	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	511	1	1	1	1	1	1	1	1	1
Full Scale (FS)	3.9375	255	0	1	1	1	1	1	1	1	1
FS - 1 LSB	3.875	254	0	1	1	1	1	1	1	1	0
3/4 FS	3.000	192	0	1	1	0	0	0	0	0	0
1/2 FS	2.000	128	0	1	0	0	0	0	0	0	0
1/4 FS	1.000	64	0	0	1	0	0	0	0	0	0
1 LSB	0.0156	1	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0

* The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

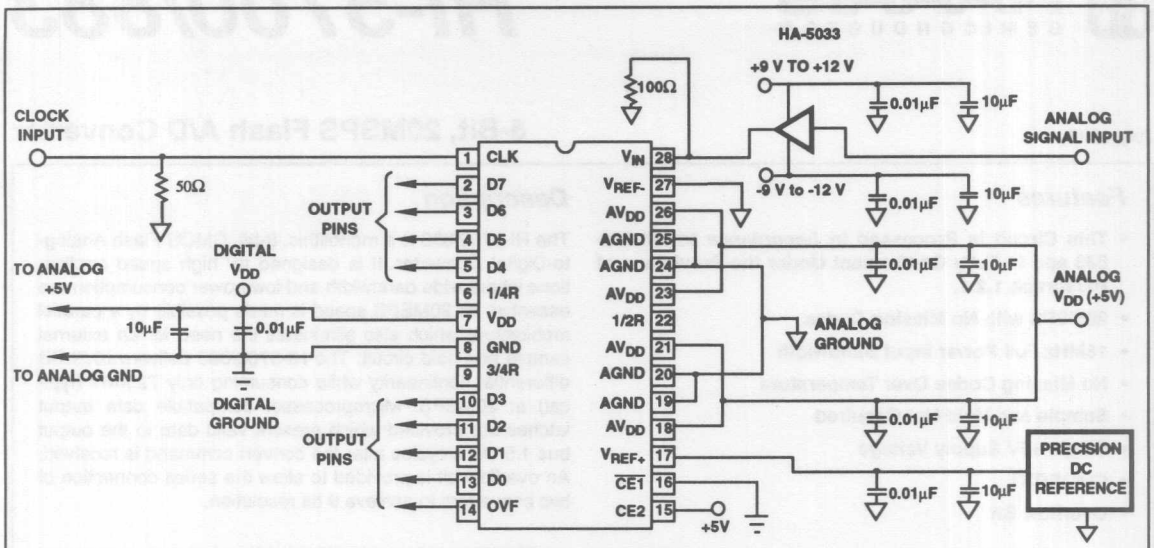


FIGURE 3. TEST CIRCUIT

Glossary of Terms

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal $\phi 1$ and $\phi 2$ clock path delays and variation between the individual comparator switching times.

Differential Linearity Error (DNL): The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1.0LSB. The range of values possible is from -1.0LSB (which implies a missing code) to greater than +1.0LSB.

Full Power Input Bandwidth: Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error (FSE): Full Scale Error is the difference between the actual input voltage of the 254 to 255 code transition and the ideal value of V_{REF+} - 1.5LSB. This error is expressed in LSBs.

Integral Linearity Error (INL): The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB: Least Significant Bit = (V_{REF+} - V_{REF-})/256. All HI-5700 specifications are given for a 15.6mV LSB size V_{REF+} = 4.0V, V_{REF-} = 0.0V.

Offset Error (VOS): Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of V_{REF-} + 0.5LSB, V_{OS} Error is expressed in LSBs.

Power Supply Rejection Ratio (PSRR): PSRR is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 254 to 255 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio (SNR): SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio (SINAD): SINAD is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion (THD): THD is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency.

HARRIS SEMICONDUCTOR

HI-5700/883

July 1992

8-Bit, 20MSPS Flash A/D Converter

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **20MSPS with No Missing Codes**
- **18MHz Full Power Input Bandwidth**
- **No Missing Codes Over Temperature**
- **Sample and Hold Not Required**
- **Single +5V Supply Voltage**
- **CMOS/TTL**
- **Overflow Bit**

Applications

- **Video Digitizing**
- **Radar Systems**
- **Medical Imaging**
- **Communication Systems**
- **High Speed Data Acquisition Systems**

Description

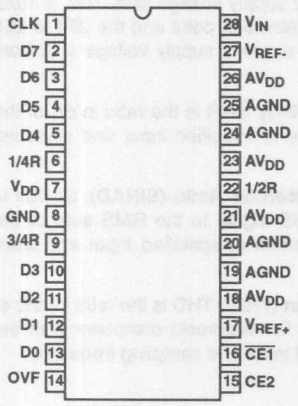
The HI-5700/883 is a monolithic, 8-bit, CMOS Flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 20MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5700/883 delivers ±0.5LSB differential nonlinearity while consuming only 725mW (typical) at 20MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 9 bit resolution.

Ordering Information

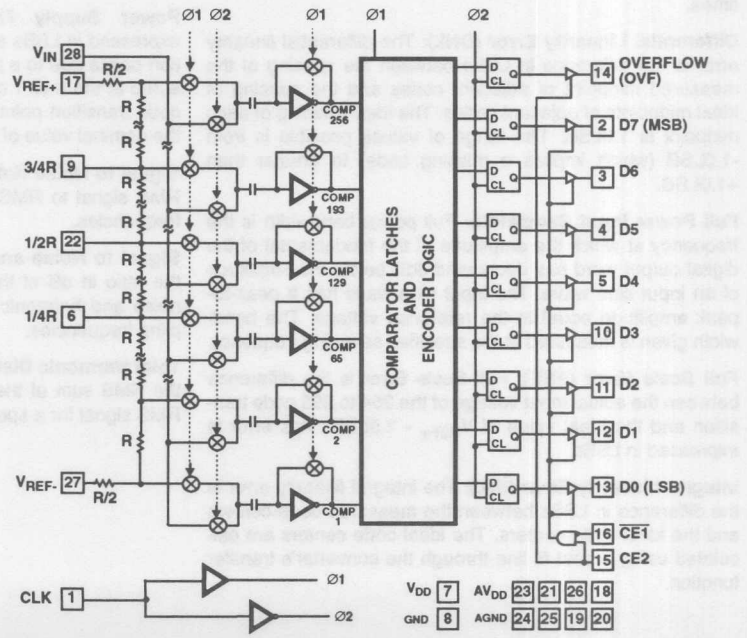
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5700S/883	-55°C to +125°C	28 Pin CERDIP

Pinout

28 PIN CERCIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3286**

Pin Descriptions

PIN #	NAME	DESCRIPTION
1	CLK	Clock Input
2	D7	Bit 7, Output (MSB)
3	D6	Bit 6, Output
4	D5	Bit 5, Output
5	D4	Bit 4, Output
6	1/4R	1/4th Point of Reference Ladder
7	V_{DD}	Digital Power Supply
8	GND	Digital Ground
9	3/4R	3/4th Point of Reference Ladder
10	D3	Bit 3, Output
11	D2	Bit 2, Output
12	D1	Bit 1, Output
13	D0	Bit 0, Output (LSB)
14	OVF	Overflow, Output
15	CE2	Three State Output Enable Input, Active High. (See Truth Table)
16	CE1	Three State Output Enable Input, Active Low. (See Truth Table))
17	V_{REF+}	Reference Voltage Positive Input
18	AV_{DD}	Analog Power Supply, +5V
19	AGND	Analog Ground
20	AGND	Analog Ground
21	AV_{DD}	Analog Power Supply, +5V
22	1/2R	1/2 Point of Reference Ladder
23	AV_{DD}	Analog Power Supply, +5V
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Analog Power Supply, +5V
27	V_{REF-}	Reference Voltage Negative Input
28	V_{IN}	Analog Input

Chip Enable Truth Table

CE1	CE2	D0 - D7	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care.

Absolute Maximum Ratings

Supply Voltage, V_{DD} to GND ..... (GND - 0.5) < V_{DD} < +7.0V
Analog and Reference Input Pins.. (V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)
Digital I/O Pins ..... (GND - 0.5) < $V_{I/O}$ < (V_{DD} +0.5V)
Operating Temperature Range
HI1-5700S/883 ..... -55°C to +125°C
Junction Temperature..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
ESD Clasification ..... Class 1

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
HI1-5700S/883	47°C/W	28°C/W

Power Dissipation at +75°C (Note 1)
HI1-5700S/883 ..... 2100mW
Power Dissipation Derating Factor Above +75°C
HI1-5700S/883 ..... 21mW/°C
Reliabiliy Information
Transistor Count 14677
Worst Case Density ..... 3.05 x 10^4 A/cm^2

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency @ 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

DC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
ACCURACY							
Integral Linearity Error (Best Fit Method)	INL	F_S = 15MHz, f_{in} = DC	1	+25°C	-	±2.0	LSB
			2, 3	+125°C, -55°C	-	±2.65	LSB
		F_S = 20MHz, f_{in} = DC	1	+25°C	-	±2.25	LSB
			2, 3	+125°C, -55°C	-	±4.1	LSB
Differential Linearity Error (Guaranteed No Missing Codes)	DNL	F_S = 15MHz, f_{in} = DC	1	+25°C	-	±0.9	LSB
			2, 3	+125°C, -55°C	-	±1.0	LSB
		F_S = 20MHz, f_{in} = DC	1	+25°C	-	±0.9	LSB
			2, 3	+125°C, -55°C	-	±1.0	LSB
Offset Error (Adjustable to zero)	VOS	F_S = 15MHz, f_{in} = DC	1	+25°C	-	±8.0	LSB
			2, 3	+125°C, -55°C	-	±9.5	LSB
		F_S = 20MHz, f_{in} = DC	1	+25°C	-	±8.0	LSB
			2, 3	+125°C, -55°C	-	±9.5	LSB
Full Scale Error (Adjustable to zero)	FSE	F_S = 15MHz, f_{in} = DC	1	+25°C	-	±4.5	LSB
			2, 3	+125°C, -55°C	-	±8.0	LSB
		F_S = 20MHz, f_{in} = DC	1	+25°C	-	±4.5	LSB
			2, 3	+125°C, -55°C	-	±8.0	LSB
ANALOG INPUT							
Analog Input Resistance	R_{IN}	V_{IN} = 4V	1	+25°C	4	-	MΩ
			2, 3	+125°C, -55°C	4	-	MΩ
Analog Input Bias Current	I_B	V_{IN} = 0V, 4V	1	+25°C		±1.0	µA
			2, 3	+125°C, -55°C		±1.0	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency @ 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

DC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
REFERENCE INPUT							
Total Reference Resistance	R_L		1	+25°C	250	-	Ω
			2, 3	+125°C, -55°C	235	-	Ω
DIGITAL INPUTS							
Input High Voltage	V_{IH}		1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
Input Low Voltage	V_{IL}		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 0V, +5V	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±1	µA
DIGITAL OUTPUTS							
Output Leakage	I_{OZ}	CE2 = 0V, V_O = 0V, 5V	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±1.0	µA
Output Logic Source Current	I_{OH}	V_O = 4.5V	1	+25°C	-3.2	-	mA
			2, 3	+125°C, -55°C	-3.2	-	mA
Output Logic Sink Current	I_{OL}	V_O = 0.4V	1	+25°C	3.2	-	mA
			2, 3	+125°C, -55°C	3.2	-	mA
POWER SUPPLY REJECTION							
Offset Error PSRR	ΔVOS	V_{DD} = 5V ±10%	1	+25°C	-	±2.75	LSB
			2, 3	+125°C, -55°C	-	±5.5	LSB
Gain Error PSRR	ΔFSE	V_{DD} = 5V ±10%	1	+25°C	-	±2.75	LSB
			2, 3	+125°C, -55°C	-	±5.5	LSB
POWER SUPPLY CURRENT							
Supply Current	I_{DD}	F_S = 20MHz	1	+25°C	-	180	mA
			2, 3	+125°C, -55°C	-	190	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency @ 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

AC PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNIT
					MIN	MAX	
Maximum Conversion Rate		No Missing Codes	9	+25°C	20	-	MSPS
			10, 11	+125°C, -55°C	20	-	MSPS
Data Output Enable Time	t_{EN}		9	+25°C	-	25	ns
			10, 11	+125°C, -55°C	-	30	ns
Data Output Disable Time	t_{DIS}		9	+25°C	-	20	ns
			10, 11	+125°C, -55°C	-	25	ns
Data Output Delay	t_{OD}		9	+25°C	-	25	ns
			10, 11	+125°C, -55°C	-	30	ns
Data Output Hold	t_H		9	+25°C	10	-	ns
			10, 11	+125°C, -55°C	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency @ 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	TEMPERAUTRE	LIMITS		UNIT
				MIN	MAX	
Minimum Conversion Rate		No missing codes	+25°C, +125°C, -55°C	-	0.125	MSPS

NOTE:

2. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Timing Waveforms

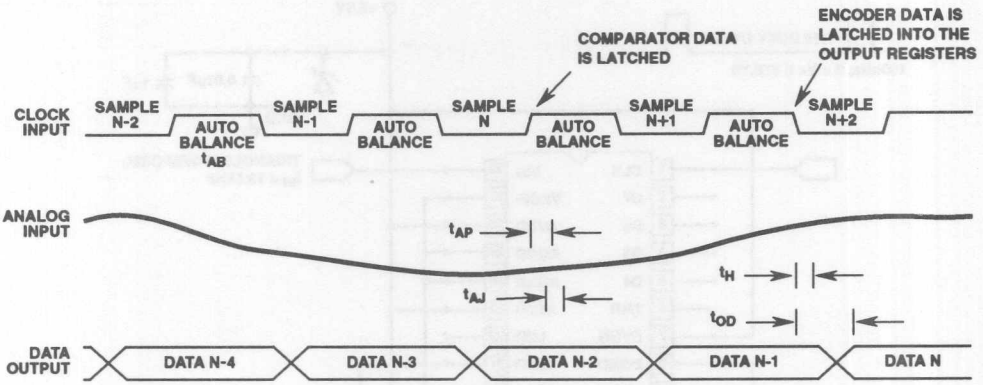


FIGURE 1. INPUT-TO-OUTPUT TIMING

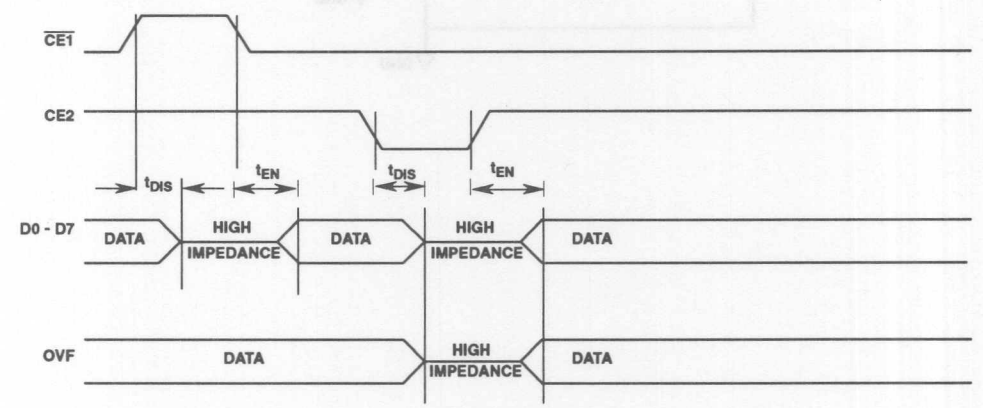
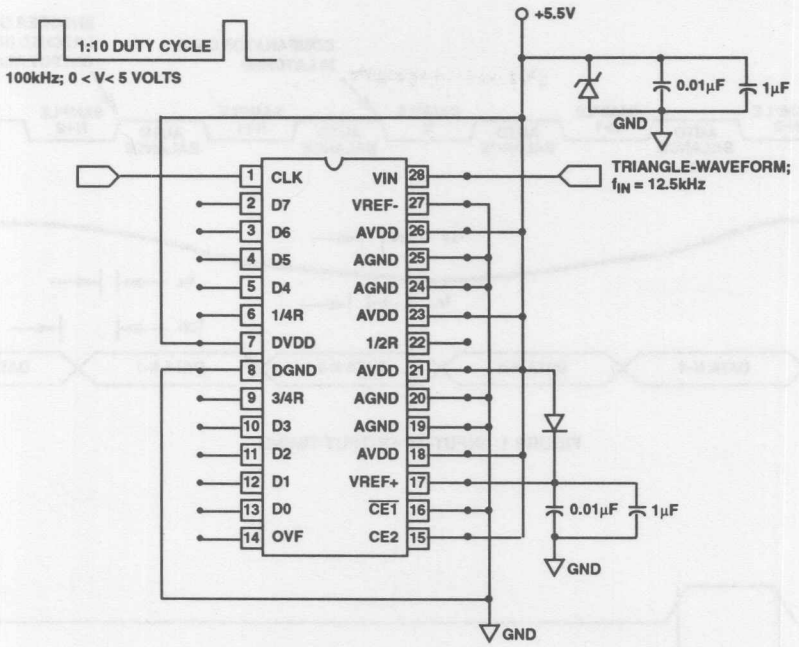


FIGURE 2. OUTPUT ENABLE TIMING

Burn-In Circuit

HI-5700/883 CERAMIC DIP



Metallization Topology

DIE DIMENSIONS:
154.3 x 173.2 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

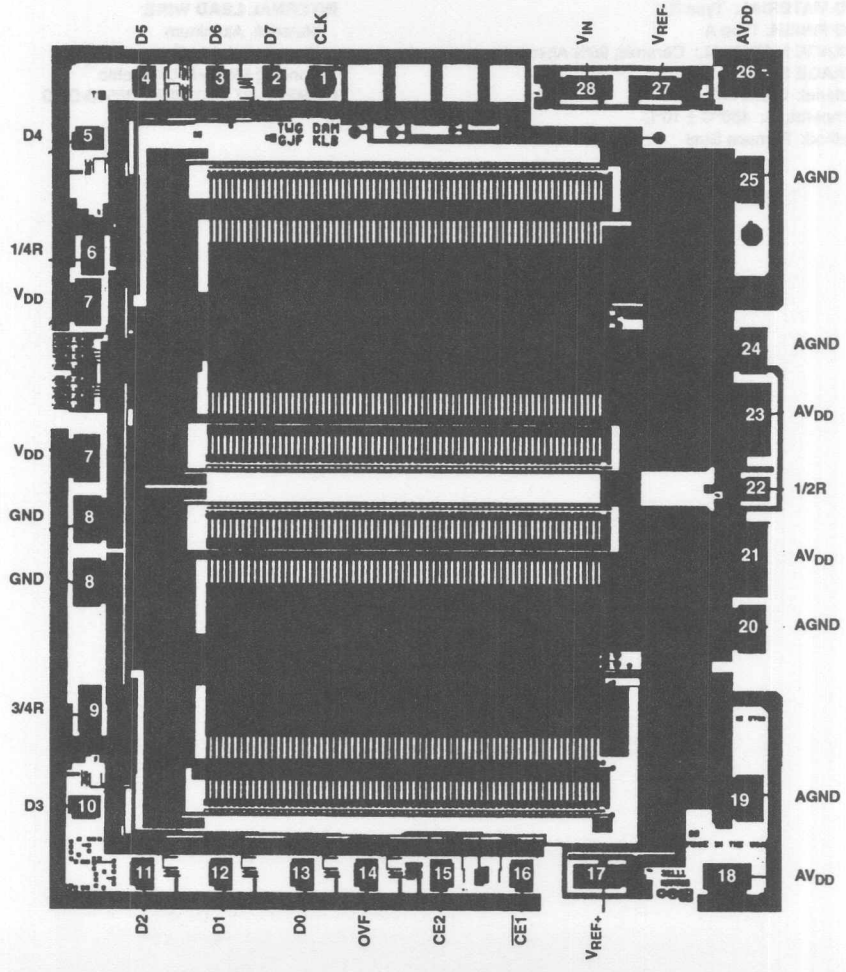
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP - 460°C (Max)

WORST CASE CURRENT DENSITY:
3.05×10^4 A/cm^2

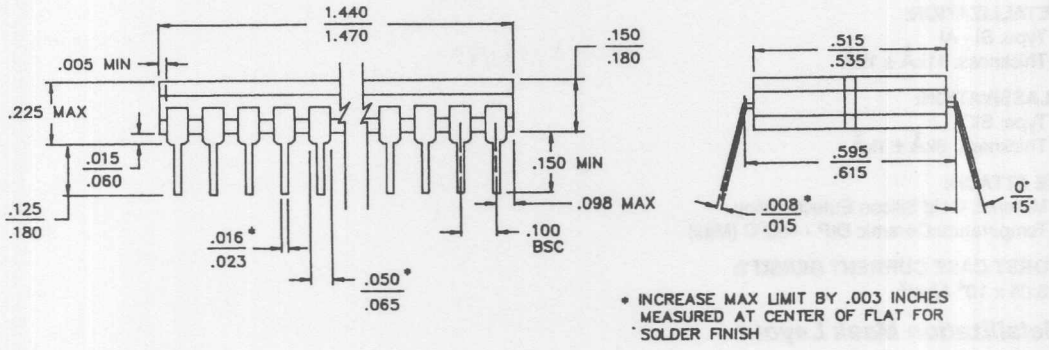
Metallization Mask Layout

HI-5700/883



Packaging†

28 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510-D-10

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes and Dimensions

HARRIS SEMICONDUCTOR

HI-5701

July 1992

6 Bit, 30 MSPS Flash A/D Converter

Features

- 30 MSPS with No Missing Codes
- 20MHz Full Power Input Bandwidth
- No Missing Codes Over Temperature
- Sample and Hold Not Required
- Single +5V Supply Voltage
- 300mW (Max) Power Dissipation
- CMOS/TTL Compatible
- Overflow Bit

Applications

- Video Digitizing
- Radar Systems
- Communication Systems
- High Speed Data Acquisition Systems

Description

The HI-5701 is a monolithic, 6 bit, CMOS flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 30 MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5701 delivers ±0.7LSB differential nonlinearity while consuming only 250mW (typical) at 30 MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 7 bit resolution.

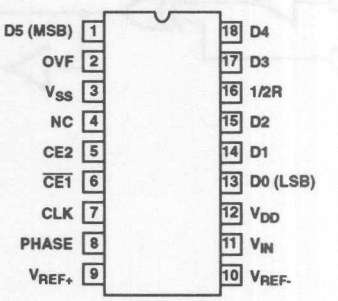
The HI-5701 is available in Commercial and Industrial temperature ranges and is supplied in 18 pin Plastic DIP and SOIC packages.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-5701K-5	0°C to +75°C	18 Pin Plastic DIP
HI9P5701K-5	0°C to +75°C	18 Pin SOIC
HI3-5701B-9	-40°C to +85°C	18 Pin Plastic DIP
HI9P5701B-9	-40°C to +85°C	18 Pin SOIC

Pinout

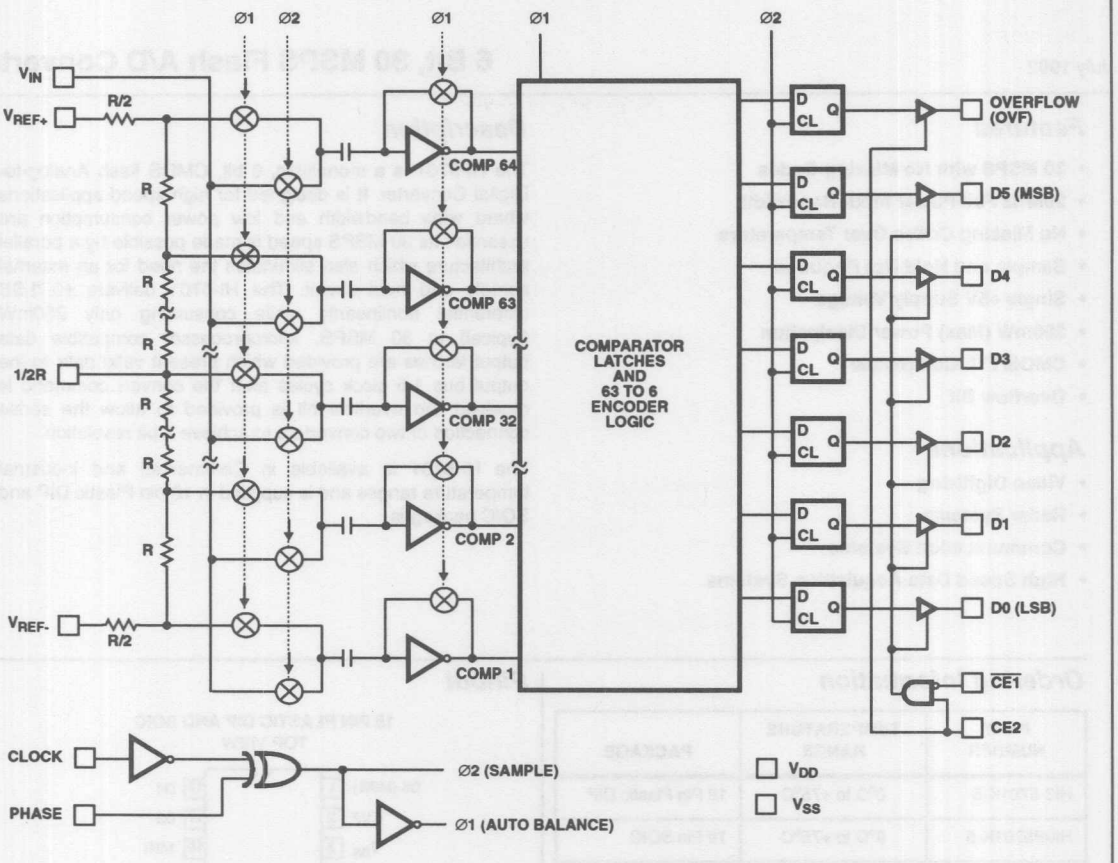
18 PIN PLASTIC DIP AND SOIC
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2937.3**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to V_{SS} ..... $(V_{SS} - 0.5) < V_{DD} < +7.0V$
Analog and Reference Input Pins..... $(V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)$
Digital I/O Pins ..... $(V_{SS} - 0.5) < V_{I/O} < (V_{DD} +0.5V)$
Operating Temperature Range
HI3-5701-5 ..... 0°C to +75°C
HI9P5701-9 ..... -40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
HI3-5701	75°C/W	26°C/W
HI9P5701	95°C/W	26°C/W

Power Dissipation at +75°C (Note 1)
HI3-5701-5 ..... 1000mW
HI9P5701-9 ..... 790mW
Power Dissipation Derating Factor Above +75°C
HI3-5701-5 ..... 13mW/°C
HI9P5701-9 ..... 10.5mW/°C

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications: V_{DD} = +5.0V; V_{REF+} = +4.0V; V_{REF-} = V_{SS} = GND; F_S = Specified Clock Frequency @ 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified.

PARAMETER	TEST CONDITION	+25°C			(NOTE 2) 0°C to +75°C -40°C to +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
SYSTEM PERFORMANCE							
Resolution		6			6		Bits
Integral Linearity Error (INL) (Best Fit Line)	F_S = 20MHz F_S = 30MHz		±0.5 ±1.5	±1.25		±2.0	LSB LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	F_S = 20MHz F_S = 30MHz		±0.3 ±0.7	±0.6		±0.75	LSB LSB
Offset Error (VOS) (Adjustable to Zero)	F_S = 20MHz (Note 2) F_S = 30MHz		±0.5 ±0.5	±2.0		±2.5	LSB LSB
Full Scale Error (FSE) (Adjustable to Zero)	F_S = 20MHz (Note 2) F_S = 30MHz		±0.25 ±0.25	±2.0		±2.5	LSB LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	30	40		30		MSPS
Minimum Conversion Rate	No Missing Codes (Note 2)			0.125		0.125	MSPS
Full Power Input Bandwidth	F_S = 30MHz		20				MHz
Signal to Noise Ratio (SNR) = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	F_S = 1MHz, f_{IN} = 100kHz F_S = 30MHz, f_{IN} = 4MHz		36 31				dB dB
Signal to Noise Ratio (SINAD) = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	F_S = 1MHz, f_{IN} = 100kHz F_S = 30MHz, f_{IN} = 4MHz		35 30				dB dB
Total Harmonic Distortion	F_S = 1MHz, f_{IN} = 100kHz F_S = 30MHz, f_{IN} = 4MHz		-44 -38				dBc dBc
Differential Gain	F_S = 14.32MHz, f_{IN} = 3.58MHz		2				%
Differential Phase	F_S = 14.32MHz, f_{IN} = 3.58MHz		2				Degree
ANALOG INPUT							

Electrical Specifications: V_{DD} = +5.0V; V_{REF+} = +4.0V; V_{REF-} = V_{SS} = GND; F_S = Specified Clock Frequency @ 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	+25°C			(NOTE 2) 0°C to +75°C -40°C to +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Analog Input Resistance, R_{IN}	V_{IN} = 4V		30				MΩ
Analog Input Capacitance, C_{IN}	V_{IN} = 0V		20				pF
Analog Input Bias Current, IB	V_{IN} = 0V, 4V		0.01	±1.0		±1.0	µA
REFERENCE INPUT							
Total Reference Resistance, R_L		250	370		235		Ω
Reference Resistance Tempco, T_C			+0.266				Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0			2.0		V
Input Logic Low Voltage, V_{IL}				0.8		0.8	V
Input Logic High Current, I_{IH}	V_{IN} = 5V			1.0		1.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V			1.0		1.0	µA
Input Capacitance, C_{IN}			7				pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2			3.2		mA
Output Logic Source Current, I_{OH}	V_O = 4.5V	-3.2			-3.2		mA
Output Leakage, I_{OFF}	CE2 = 0V			±1.0		±1.0	µA
Output Capacitance, C_{OUT}	CE2 = 0V		5.0				pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}			6				ns
Aperture Jitter, t_{AJ}			30				ps
Data Output Enable Time, t_{EN}	(Note 2)		12	20		20	ns
Data Output Disable Time, t_{DIS}	(Note 2)		11	20		20	ns
Data Output Delay, t_{OD}	(Note 2)		14	20		20	ns
Data Output Hold, t_H	(Note 2)	5	10		5		ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔVOS	V_{DD} = 5V ± 10%		±0.1	±1.0		±1.5	LSB
Gain Error PSRR, ΔFSE	V_{DD} = 5V± 10%		±0.1	±1.0		±1.5	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	F_S = 30MHz		50	60		75	mA

NOTE:

2. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

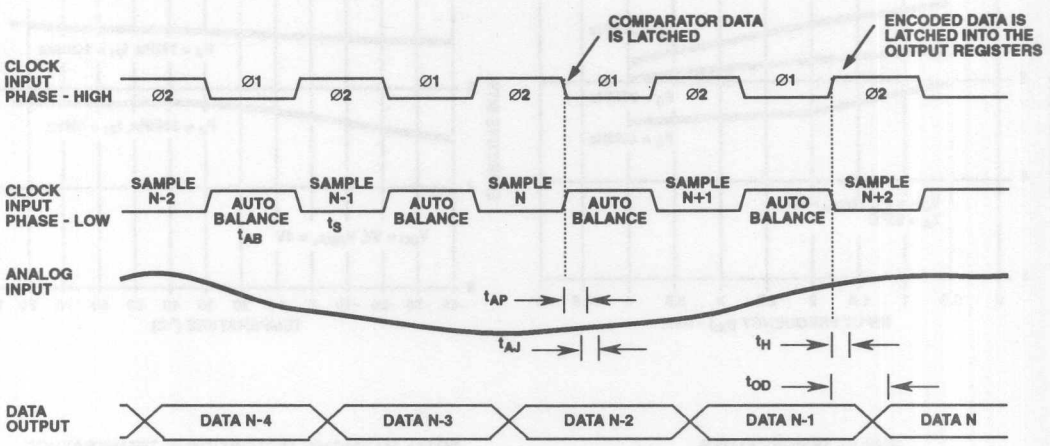


FIGURE 1. INPUT-TO-OUTPUT TIMING

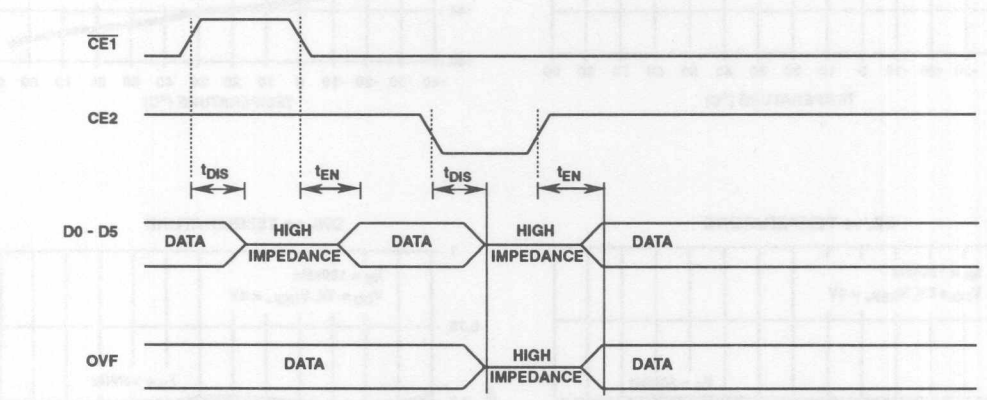
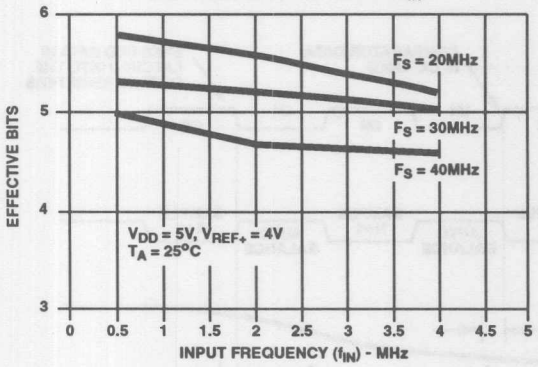


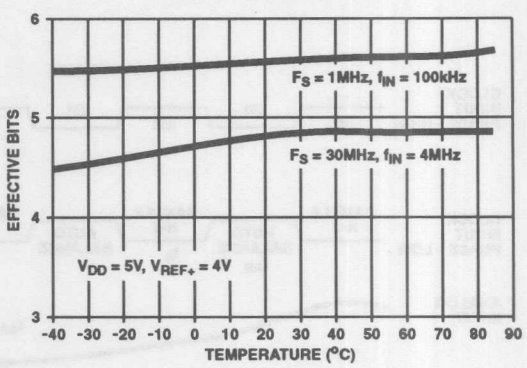
FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

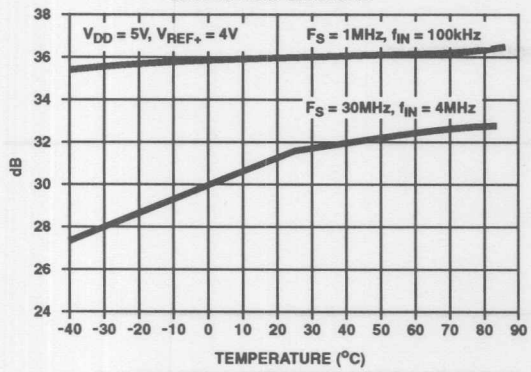
EFFECTIVE NUMBER OF BITS vs f_{IN}



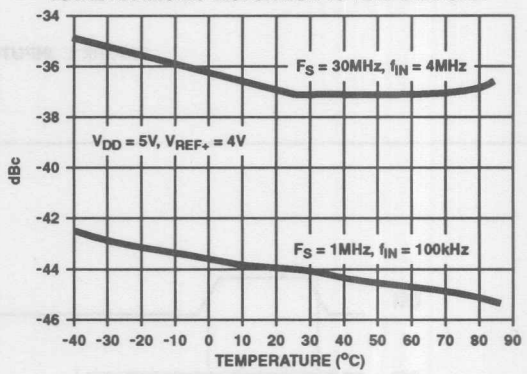
ENOB vs TEMPERATURE



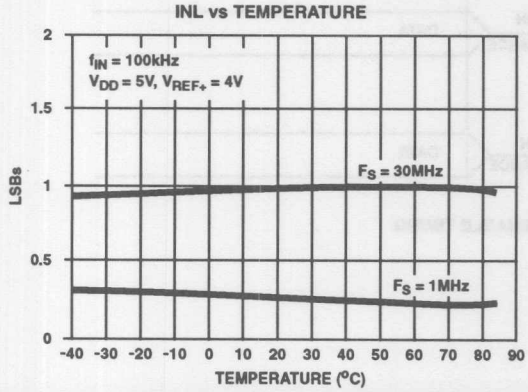
SNR vs TEMPERATURE



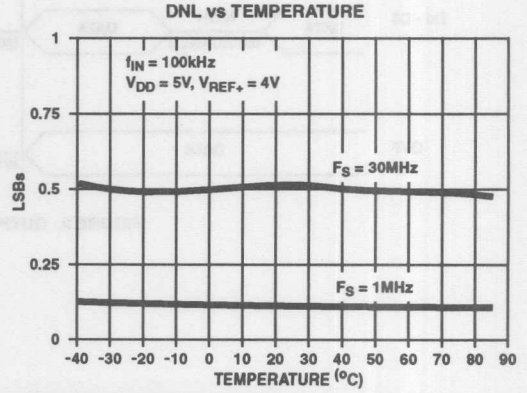
TOTAL HARMONIC DISTORTION vs TEMPERATURE



INL vs TEMPERATURE

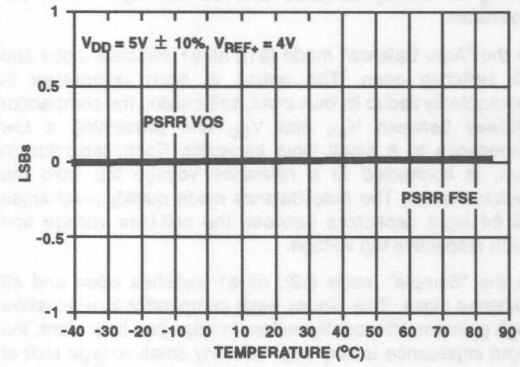


DNL vs TEMPERATURE

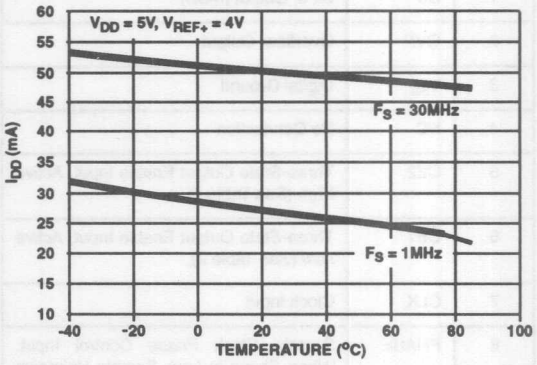


Typical Performance Curves (Continued)

POWER SUPPLY REJECTION vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs CLOCK AND DUTY CYCLE

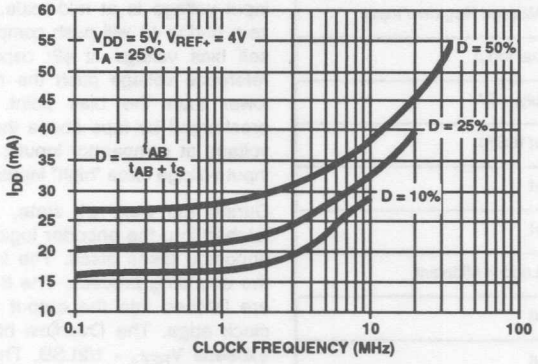


TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	D5	Bit 6, Output (MSB)
2	OVF	Overflow, Output
3	V_{SS}	Digital Ground
4	NC	No Connection
5	CE2	Three-State Output Enable Input, Active High (See Table 2).
6	$\overline{CE1}$	Three-State Output Enable Input, Active Low (See Table 2).
7	CLK	Clock Input
8	PHASE	Sample Clock Phase Control Input. When Phase is Low, Sample Unknown (ϕ1) Occurs When the Clock is Low and Auto Balance (ϕ2) Occurs When the Clock is High (See Text).
9	V_{REF+}	Reference Voltage Positive Input
10	V_{REF-}	Reference Voltage Negative Input
11	V_{IN}	Analog Signal Input
12	V_{DD}	Power Supply, +5V
13	D0	Bit 1, Output (LSB)
14	D1	Bit 2, Output
15	D2	Bit 3, Output
16	1/2 R2	Reference Ladder Midpoint
17	D3	Bit 4, Output
18	D4	Bit 5, Output

Theory of Operation

The HI-5701 is a 6 bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 64 comparators are used in the HI-5701; 63 comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5701 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5701 CMOS flash converter operates.

The input clock which controls the operation of the HI-5701 is first split into a non-inverting ϕ1 clock and an inverting ϕ2 clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto Balance" mode (ϕ1), all ϕ1 switches close and ϕ2 switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between V_{SS} and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 64 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode (ϕ2), all ϕ1 switches open and ϕ2 switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The ϕ2 state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 64 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during ϕ1 will push comparator inputs higher than the self bias voltage at ϕ2; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next ϕ1 state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following ϕ2 state completes the encoding process. The 6 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds V_{REF+} - 1/2LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second ϕ1 state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the ϕ1 state. Refer to the Glossary of Terms for other definitions.

Applications Information

Voltage Reference

The reference voltage is applied across the resistor ladder at the input of the converter, between V_{REF+} and V_{REF-}. In most applications, V_{REF-} is simply tied to analog ground such that the reference source drives V_{REF+}. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235 Ohms over temperature.

The HI-5701 is specified for a reference voltage of 4.0 volts, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0 volt reference operation, the converter encodes the analog input into a binary output in LSB increments of $(V_{REF+} - V_{REF-})/64$, or 62.5mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2 volts. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01µF and 10µF) capacitors near the package pin are recommended. It is not necessary to decouple the 1/2R tap point pin for most applications.

It is possible to elevate V_{REF-} from ground if necessary. In this case, the V_{REF-} pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5701 provides a standard high speed interface to external CMOS and TTL logic families. Four digital inputs are provided to control the function of the converter. The clock and phase inputs control the sample and auto balance modes. The digital outputs change state on the clock phase which begins the sample mode. Two chip enable inputs control the three-state outputs of output bits D0 through D5 and the Overflow OVF bit. As indicated in Table 2, all output bits are high impedance when CE2 is low, and output bits D0 through D5 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local ground disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the "Theory of Operation" section. The Auto Balance $\phi1$ half cycle of the clock may be reduced to 16ns; the Sample $\phi2$ half cycle may be varied from a minimum of 16ns to a maximum of 8µs.

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D5	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

TABLE 3. PHASE CONTROL

CLOCK	PHASE	INTERNAL GENERATION
0	0	Sample Unknown ($\phi2$)
0	1	Auto Balance ($\phi1$)
1	0	Auto Balance ($\phi1$)
1	1	Sample Unknown ($\phi2$)

Gain and Offset Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and midpoint trim. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

The preferred offset correction method is to introduce a DC component to V_{IN} of the converter. An alternate method is to adjust the V_{REF-} input to produce the desired offset adjustment. The theoretical input voltage to produce the first transition is 1/2LSB.

$$V_{IN} \text{ (0 to 1 transition)} = 1/2LSB = 1/2(V_{REF}/64) = V_{REF}/128$$

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the V_{REF+} input voltage. This adjustment is performed by setting V_{IN} to the 63 to overflow transition. The theoretical input voltage to produce the transition is 1/2LSB less than V_{REF+} and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - (V_{REF}/128) = V_{REF}(127/128).$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF+} until that transition occurs on the outputs.

Midpoint Trim

The reference center (1/2R) is available to the user as the midpoint of the resistor ladder. The 1/2R point can be used to improve linearity or create unique transfer functions. The offset and gain trims should be done prior to adjusting the midpoint. The theoretical transition from count 31 to 32 occurs at 31.5LSB's. That voltage is calculated as follows:

$$V_{IN} \text{ (31 to 32 transition)} = 31.5(V_{REF}/64) = V_{REF}(63/128).$$

An adjustable voltage follower can be used to drive the 1/2R pin. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower until the transition occurs on the output bits.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feed through in the capacitor array. It varies with the amplitude of the analog input and the sampling rate.

The signal source must be capable of recovering from the transient prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HFA-0005, HA-5004, HA-5002, and HA-5033.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +1/2LSB are converted to all zeros; input voltages of V_{REF+} - 1/2LSB to V_{DD} + 0.5 are converted to all ones with the Overflow bit set.

Power Supplies

The HI-5701 operates nominally from 5 volt supplies but will function from 3 volts to 6 volts. The analog supply should be well regulated and "clean" of significant noise, especially high frequency noise. It is recommended that power supply decoupling capacitors be placed as close to the supply pins as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors is recommended for this purpose as shown in the test circuit Figure 4.

Reducing Power Consumption

Power dissipation in the HI-5701 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by shortening the Auto Balance ϕ1 portion of the clock duty cycle.

TABLE 4. OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* V_{REF+} = 4.0V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB						LSB
			OVF	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	127	1	1	1	1	1	1	1
Full Scale (FS)	3.9375	63	0	1	1	1	1	1	1
FS - 1LSB	3.875	62	0	1	1	1	1	1	0
	•					•			
	•					•			
	•					•			
3/4 FS	3.000	48	0	1	1	0	0	0	0
	•					•			
	•					•			
	•					•			
1/2 FS	2.000	32	0	1	0	0	0	0	0
	•					•			
	•					•			
	•					•			
1/4 FS	1.000	16	0	0	1	0	0	0	0
	•					•			
	•					•			
	•					•			
1LSB	0.0625	1	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0

* The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Glossary of Terms

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal $\phi 1$ and $\phi 2$ clock path delays and variation between the individual comparator switching times.

Differential Linearity Error (DNL): The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1.0LSB. The range of values possible is from -1.0LSB (which implies a missing code) to greater than +1.0LSB.

Full Power Input Bandwidth: Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error (FSE): Full Scale Error is the difference between the actual input voltage of the 63 to 64 code transition and the ideal value of V_{REF+} - 1.5LSB. This error is expressed in LSBs.

Integral Linearity Error (INL): The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB: Least Significant Bit = (V_{REF+} - V_{REF-})/64. All HI-5701 specifications are given for a 62.5mV LSB size V_{REF+} = 4.0V, V_{REF-} = 0.0V.

Offset Error (VOS): Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of V_{REF-} + 0.5LSB. VOS error is expressed in LSBs.

Power Supply Rejection Ratio (PSRR): PSRR is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 62 to 63 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio (SNR): SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio (SINAD): SINAD is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion (THD): THD is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency.

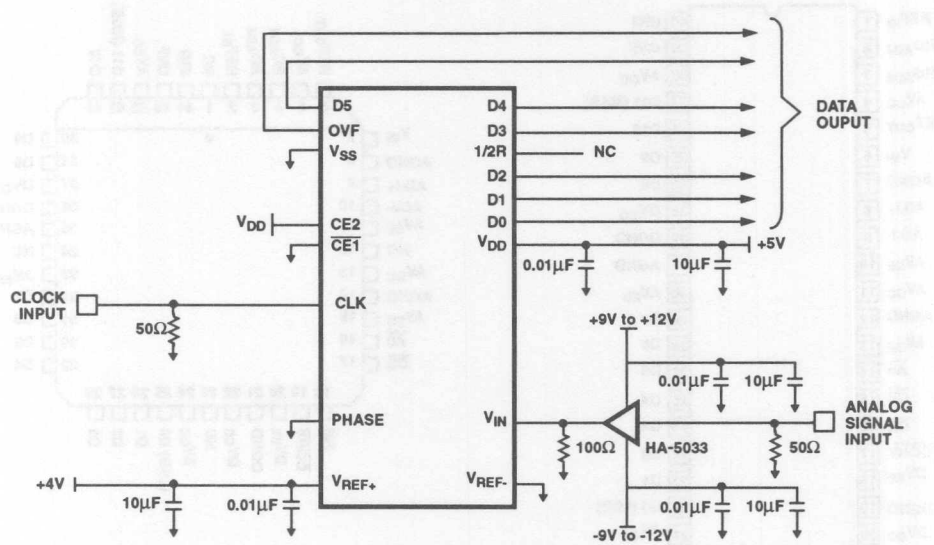


FIGURE 3. TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI5800

PRELIMINARY

July 1992

12-Bit, 3MSPS Sampling A/D Converter

Features

- 3MSPS Throughput Rate
- 12-Bit, No Missing Codes over Temperature
- 1.0LSB Integral Linearity Error
- Buffered Sample and Hold Amplifier
- Precision Voltage Reference
- ± 2.5V Input Signal Range
- 20MHz Input BW Allows Sampling Beyond Nyquist
- Zero Latency/No Pipeline Delay

Applications

- High Speed Data Acquisition Systems
- Medical Imaging
- Radar Signal Analysis
- Document and Film Scanners
- Vibration/Waveform Spectrum Analysis
- Digital Servo Control

Description

The HI5800 is a monolithic, 12-bit, sampling Analog-to-Digital Converter fabricated in the HBC10 BiCMOS process. It is a complete subsystem containing a sample and hold amplifier, voltage reference, two-step subranging A/D, error correction, control logic, and timing generator. The HI5800 is designed for high speed applications where wide bandwidth, accuracy and low distortion are essential.

The HI5800 is available in Commercial and Industrial temperature ranges and is offered in a 40 pin Sidebraze and a 44 pin PLCC package.

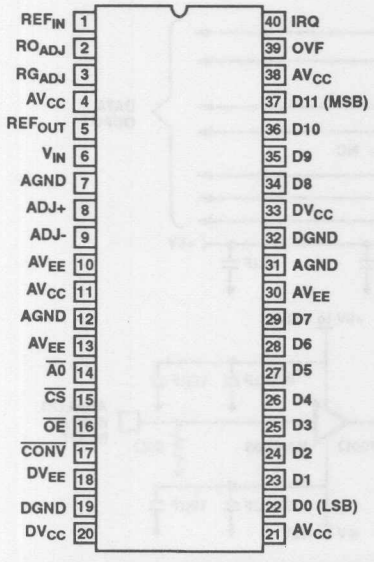
Ordering Information

PART NUMBER	LINEARITY	TEMP. RANGE	PACKAGE
HI5800AID HI5800BID	±2LSB ±1LSB	-40°C to +85°C	40 Pin Sidebraze
HI5800JCM* HI5800KCM*	±2LSB ±1LSB	0°C to +75°C	44 Pin PLCC

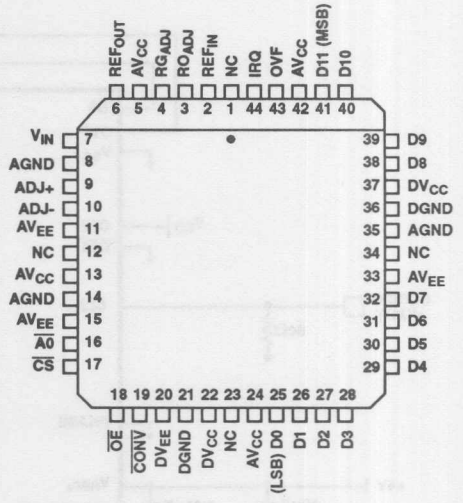
* Consult factory for availability

Pinouts

40 PIN SIDEBRAZE
TOP VIEW



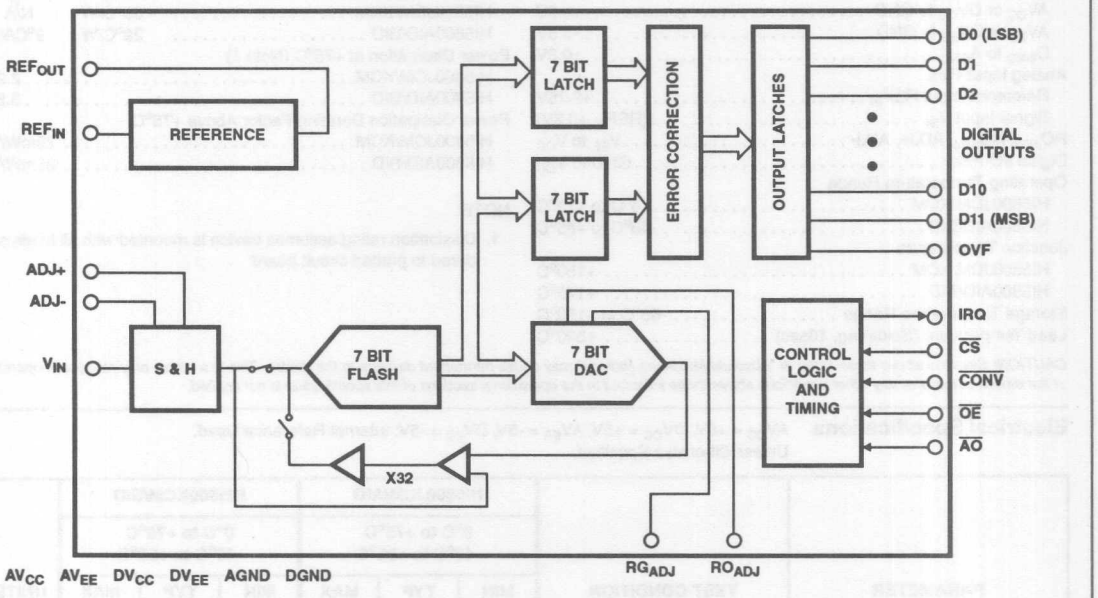
44 PIN PLCC
TOP VIEW



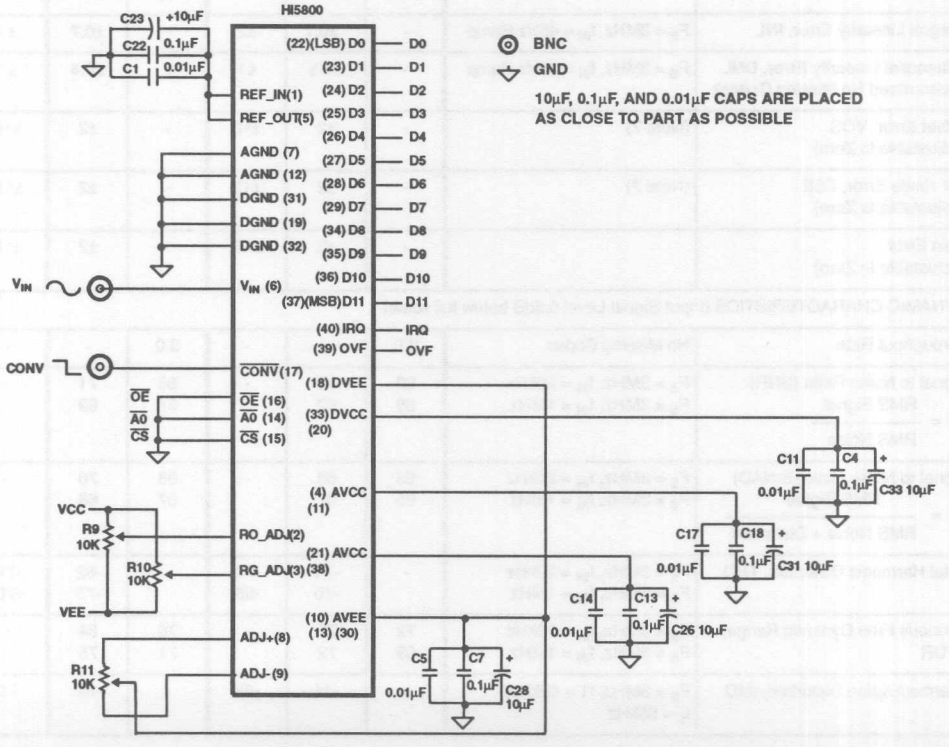
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2938.1

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltages
- AV_{CC} or DV_{CC} to GND ..... +5.5V
- AV_{EE} or DV_{EE} to GND ..... -5.5V
- D_{GND} to A_{GND} ..... ±0.3V

Analog Input Pins
- Reference Input REF_{IN} ..... +2.75V
- Signal Input V_{IN} ..... ±(REF_{IN} +0.2V)

RO_{ADJ}, RG_{ADJ}, ADJ+, ADJ- ..... V_{EE} to V_{CC}

Digital I/O Pins ..... GND to V_{CC}

Operating Temperature Range
- HI5800JCM/KCM ..... 0°C to +75°C
- HI5800AID/BID ..... -40°C to +85°C

Junction Temperature
- HI5800JCM/KCM ..... +150°C
- HI5800AID/BID ..... +175°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10sec) ..... +300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
HI5800JCM/KCM	35°C/W	N/A
HI5800AID/BID	29°C/W	9°C/W

Power Dissipation at +75°C (Note 1)
- HI5800JCM/KCM 2.2W
- HI5800AID/BID 3.5W

Power Dissipation Derating Factor Above +75°C
- HI5800JCM/KCM ..... 29mW/°C
- HI5800AID/BID ..... 35mW/°C

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used. Unless 0therwise Specified.

PARAMETER	TEST CONDITION	HI5800JCM/AID 0°C to +75°C -40°C to +85°C MIN	TYP	MAX	HI5800KCM/BID 0°C to +75°C -40°C to +85°C MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE								
Resolution		12	-	-	12	-	-	Bits
Integral Linearity Error, INL	F_S = 3MHz, f_{IN} = 45Hz Ramp	-	±0.7	±2	-	±0.7	±1	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	F_S = 3MHz, f_{IN} = 45Hz Ramp	-	±0.5	±1	-	±0.4	±1	LSB
Offset Error, VOS (Adjustable to Zero)	(Note 7)	-	±2	±10	-	±2	±10	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 7)	-	±2	±10	-	±2	±10	LSB
Gain Error (Adjustable to Zero)		-	±2	±15	-	±2	±15	LSB
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB below full scale)								
Throughput Rate	No Missing Codes	3.0	-	-	3.0	-	-	MSPS
Signal to Noise Ratio (SNR) = RMS Signal / RMS Noise	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	66 65	69 67	-	68 67	71 69	-	dBc dBc
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	66 65	68 67	-	68 67	70 68	-	dBc dBc
Total Harmonic Distortion, THD	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	-	-74 -70	-70 -68	-	-82 -75	-74 -70	dBc dBc
Spurious Free Dynamic Range, SFDR	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	72 69	76 72	-	76 71	84 75	-	dBc dBc
Intermodulation Distortion, IMD	F_S = 3MHz, f1 = 49kHz, f_2 = 50kHz	-	-74	-68	-	-82	-70	dBc

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used. Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	HI5800JCM/AID 0°C to +75°C -40°C to +85°C			HI5800KCM/BID 0°C to +75°C -40°C to +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Differential Gain	F_S = 1MHz	-	0.9	-	-	0.9	-	%
Differential Phase	F_S = 1MHz	-	0.05	-	-	0.05	-	Degrees
Aperture Delay, t_{AD}		-	12	20	-	12	20	ns
Aperture Jitter, t_{AJ}		-	10	20	-	10	20	ps
ANALOG INPUT								
Input Voltage Range		-	±2.5	±2.7	-	±2.5	±2.7	V
Input Resistance		10	30	-	10	30	-	MΩ
Input Capacitance		-	5	-	-	5	-	pF
Input Current		-	1	±10	-	1	±10	µA
Input Bandwidth		-	20	-	-	20	-	MHz
INTERNAL VOLTAGE REFERENCE								
Reference Output Voltage, REFOUT (Loaded)		2.450	2.500	2.550	2.470	2.500	2.530	Volts
Reference Output Current	Note 5	2	-	-	2	-	-	mA
Reference Temperature Coefficient		-	20		-	20	-	ppm/°C
REFERENCE INPUT								
Reference Input Range		-	2.5	2.6	-	2.5	2.6	V
Reference Input Resistance		-	200	-	-	200	-	Ω
DIGITAL INPUTS								
Input Logic High Voltage, V_{IH}	Note 6	2.0	-	-	2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	-	0.8	V
Input Logic Current, I_{IL}	V_{IN} = 0V, 5V	-	1.0	±10	-	1	±10	µA
Digital Input Capacitance, CI_N	V_{IN} = 0V	-	5.0	-	-	5	-	pF
DIGITAL OUTPUTS								
Output Logic High Voltage, V_{OH}	I_{OUT} = -160µA	2.4	4.3	-	2.4	4.3	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.2mA	-	0.22	0.8	-	0.22	0.8	V
Output Logic High Current, I_{OH}		-0.160	6	-	-0.160	6	-	mA
Output Logic Low Current, I_{OL}		3.2	6	-	3.2	6	-	mA
Output 3-state Leakage Current, I_{OZ}	V_{OUT} = 0V, 5V	-	±1	±10	-	±1	±10	µA
Digital Output Capacitance, C_{OUT}		-	10	-	-	10	-	pF
TIMING CHARACTERISTICS								
Minimum $\overline{CONV}$ Pulse, t1	(Notes 2, 3)	10	-	-	10	-		ns

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used. Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	HI5800JCM/AID 0°C to +75°C -40°C to +85°C			HI5800KCM/BID 0°C to +75°C -40°C to +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{CONV}$ Setup Time, t2	(Note 2)	10	-	-	10	-		ns
$\overline{CONV}$ to $\overline{CS}$ Setup Time, t3	(Note 2)	0	-	-	0	-		ns
Minimum $\overline{OE}$ Pulse, t4	(Notes 2, 4)	15	-	-	15	-		ns
$\overline{CS}$ to $\overline{OE}$ Setup Time, t5	(Note 2)	0	-	-	0	-		ns
$\overline{OE}$ to $\overline{CS}$ Setup Time, t6	(Note 2)	0	-	-	0	-		ns
IRQ Delay from Start Convert, t7	(Note 2)	10	20	25	10	20	25	ns
IRQ Pulse Width, t8		190	205	230	190	205	230	ns
Minimum Cycle Time for Conversion, t9		-	-	333	-	333	333	ns
IRQ to Data Valid Delay, t10	(Note 2)	-5	0	+5	-5	0	+5	ns
Minimum $\overline{A0}$ Pulse, t11	(Notes 2, 4)	10	-	-	10	-	-	ns
Data Access from $\overline{OE}$ Low, t12	(Note 2)	10	18	25	10	18	25	ns
LSB, Nibble Delay from $\overline{A0}$ High, t13	(Note 2)	-	10	20	-	10	20	ns
MSB Delay from $\overline{A0}$ Low, t14	(Note 2)	-	14	20	-	14	20	ns
$\overline{CS}$ to Float Delay, t15	(Note 2)	10	18	25	10	18	25	ns
Minimum $\overline{CS}$ Pulse, t16	(Notes 2, 4)	15	-	-	15	-	-	ns
$\overline{CS}$ to Data Valid Delay, t17	(Note 2)	10	18	25	10	18	25	ns
Output Fall Time, tf	(Note 2)	-	5	20	-	5	20	ns
Output Rise Time, tr	(Note 2)	-	5	20	-	5	20	ns
POWER SUPPLY CHARACTERISTICS								
IV_{CC}		-	180	220	-	180	220	mA
IV_{EE}		-	158	190	-	158	190	mA
IDV_{CC}		-	27	40	-	27	40	mA
IDV_{EE}		-	2.7	5	-	2.7	5	mA
Power Dissipation		-	1.8	2.2	-	1.8	2.2	W
PSRR	V_{CC}, V_{EE} ±5%	-	0.01	0.05	-	0.01	0.05	%/%

NOTE:

2. Parameter guaranteed by design or characterization and not production tested.
3. Recommended pulse width for $\overline{CONV}$ is 60ns.
4. Recommended minimum pulse width is 25ns.
5. This is the additional current available from the REF_{OUT} pin with the REF_{OUT} pin driving the REF_{IN} pin.
6. The $\overline{A0}$ pin V_{IH} at -40°C may exceed 2.0V by up to 0.4V at initial power up.
7. Excludes error due to internal reference temperature drift.

Timing Diagrams

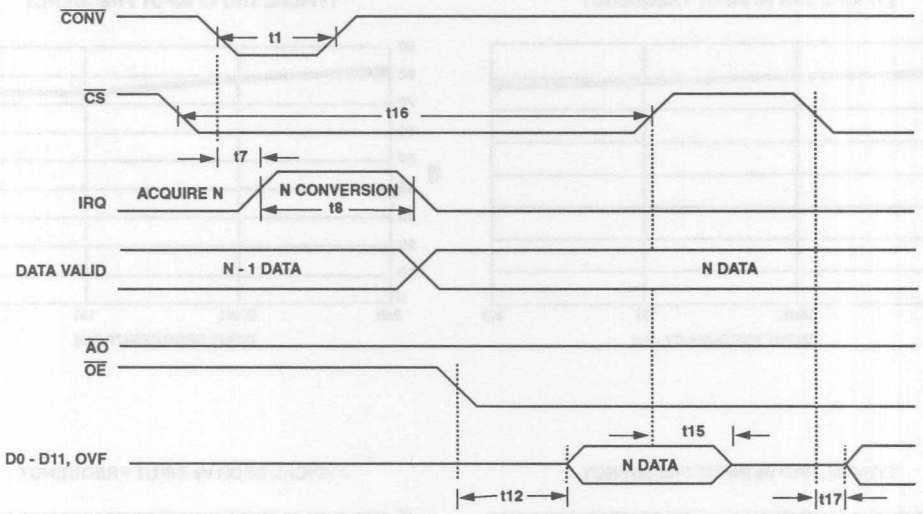


FIGURE 1. SINGLE SHOT TIMING

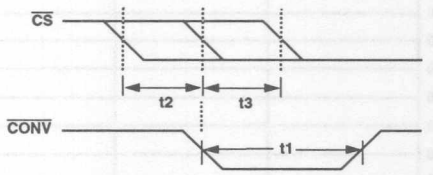


FIGURE 2A. START CONVERSION SETUP TIME

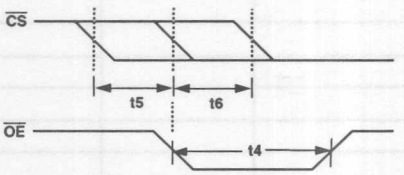


FIGURE 2B. OUTPUT ENABLE SETUP TIME

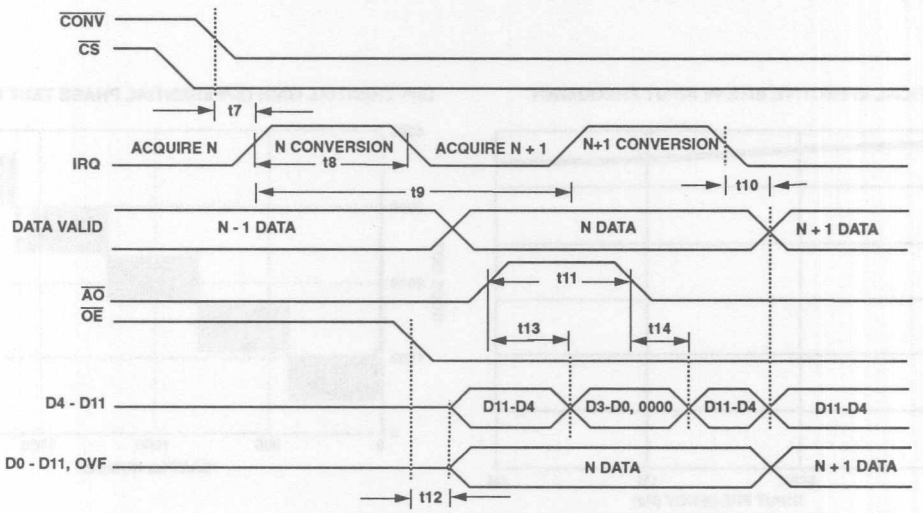
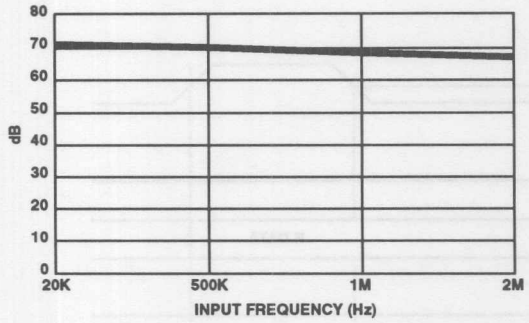


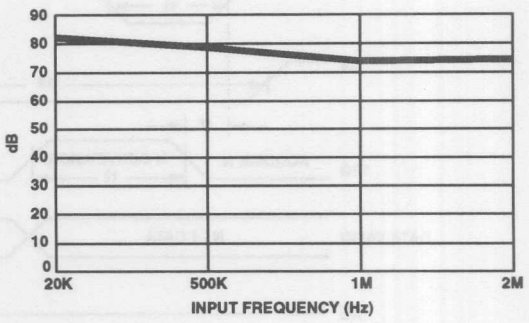
FIGURE 3. CONTINUOUS CONVERSION TIMING

Typical Performance Curves

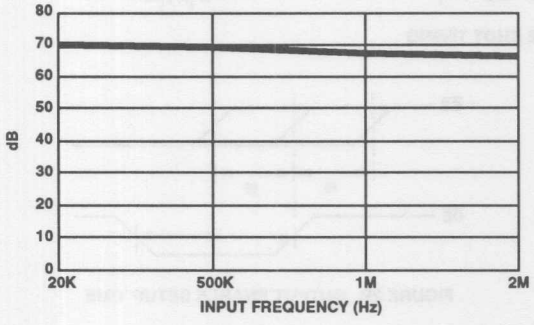
TYPICAL SNR vs INPUT FREQUENCY



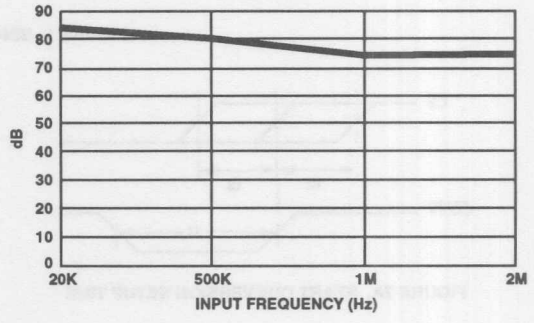
TYPICAL THD vs INPUT FREQUENCY



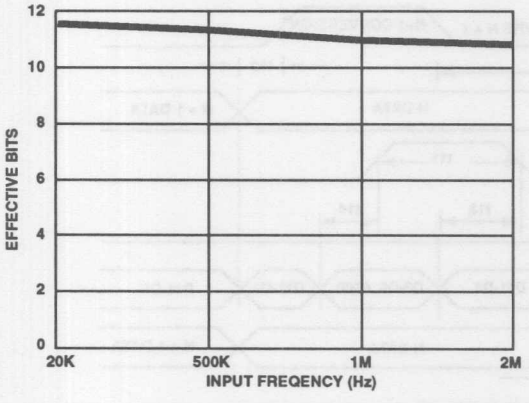
TYPICAL SND vs INPUT FREQUENCY



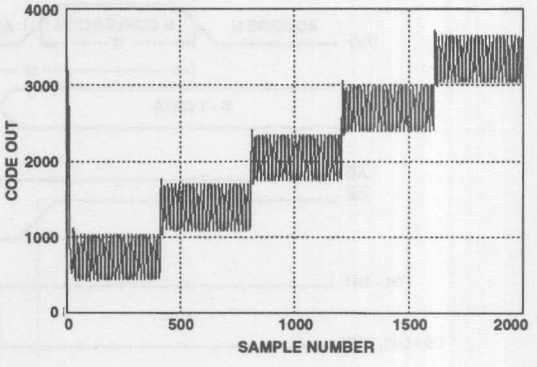
TYPICAL SPDR vs INPUT FREQUENCY



TYPICAL EFFECTIVE BITS vs INPUT FREQUENCY

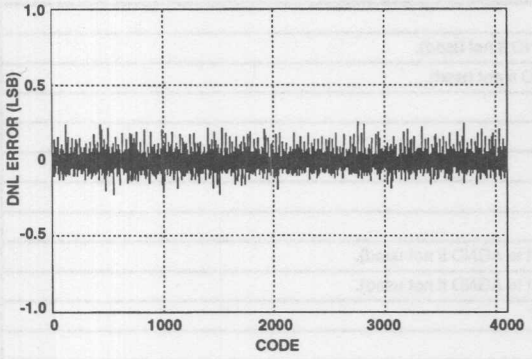


DIFFERENTIAL GAIN DIFFERENTIAL PHASE TEST OUTPUT

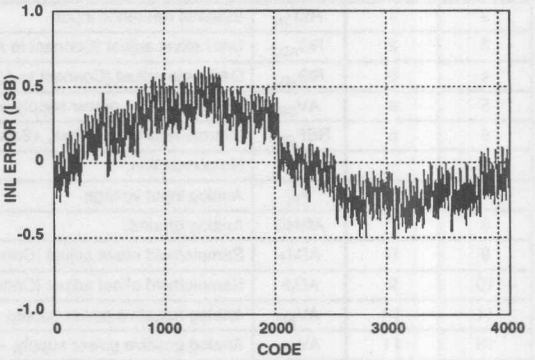


Typical Performance Curves (Continued)

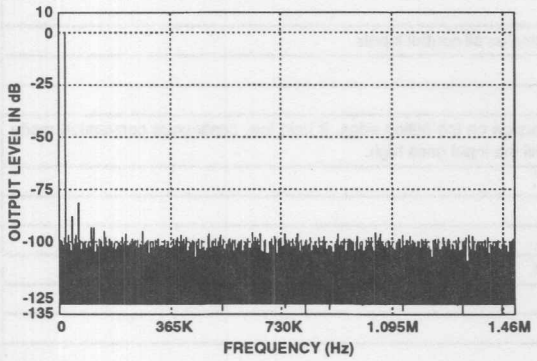
DIFFERENTIAL NON-LINEARITY



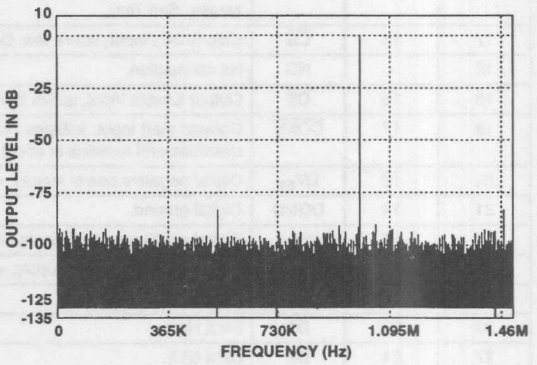
INTEGRAL NON-LINEARITY



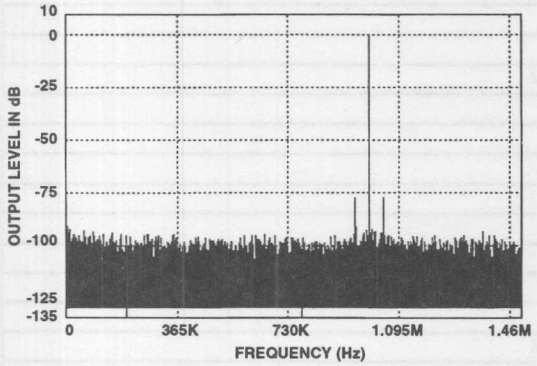
FFT SPECTRAL PLOT FOR F_{IN} = 20kHz, F_S = 3MHz



FFT SPECTRAL PLOT FOR F_{IN} = 1MHz, F_S = 3MHz



FFT SPECTRAL PLOT FOR F_{IN} = 2MHz, F_S = 3MHz



INTERMODULATION DISTORTION PLOT FOR F_{IN} = 49kHz, 50kHz at F_S = 3MHz

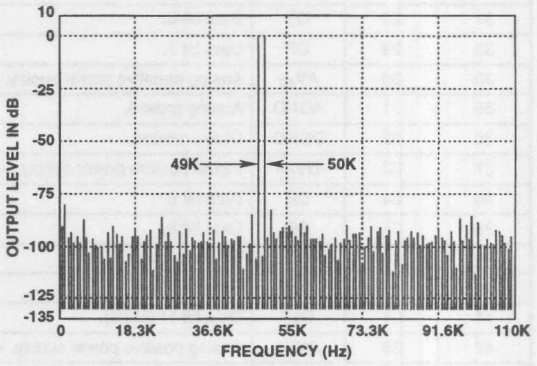


TABLE 1. PIN DESCRIPTION

44 PIN PLCC	40 PIN DIP	PIN NAME	PIN DESCRIPTION
2	1	REF_{IN}	External reference input.
3	2	RO_{ADJ}	DAC offset adjust (Connect to AGND if not used).
4	3	RG_{ADJ}	DAC gain adjust (Connect to AGND if not used).
5	4	AV_{CC}	Analog positive power supply, +5V
6	5	REF_{OUT}	Internal reference output, +2.5V.
1	-	NC	No connection.
7	6	V_{IN}	Analog input voltage.
8	7	AGND	Analog ground.
9	8	ADJ+	Sample/hold offset adjust (Connect to AGND if not used).
10	9	ADJ-	Sample/hold offset adjust (Connect to AGND if not used).
11	10	AV_{EE}	Analog negative power supply, -5V
13	11	AV_{CC}	Analog positive power supply, +5V
14	12	AGND	Analog ground.
15	13	AV_{EE}	Analog negative power supply, -5V
16	14	$\overline{A0}$	Output byte control input, active low. When low, data is presented as a 12 bit word or the upper byte (D11-D4) in 8 bit mode. When high, the second byte contains the lower LSBs (D3-D0) with 4 trailing zeroes. See Text.
17	15	$\overline{CS}$	Chip Select input, active low. Dominates all control inputs.
12	-	NC	No connection.
18	16	$\overline{OE}$	Output Enable input, active low.
19	17	$\overline{CONV}$	Convert start input. Initiates conversion on the falling edge. If held low, continuous conversion mode overrides and remains in effect until the input goes high.
20	18	DV_{EE}	Digital negative power supply, -5V.
21	19	DGND	Digital ground.
22	20	DV_{CC}	Digital positive power supply, +5V.
24	21	AV_{CC}	Analog positive power supply, +5V.
25	22	D0	Data bit 0, (LSB).
26	23	D1	Data bit 1.
27	24	D2	Data bit 2.
28	25	D3	Data bit 3.
23	-	NC	No connection
29	26	D4	Data bit 4.
30	27	D5	Data bit 5.
31	28	D6	Data bit 6.
32	29	D7	Data bit 7.
33	30	AV_{EE}	Analog negative power supply, -5V.
35	31	AGND	Analog ground.
36	32	DGND	Digital ground.
37	33	DV_{CC}	Digital positive power supply, +5V.
38	34	D8	Data bit 8.
39	35	D9	Data bit 9.
34	-	NC	No connection.
40	36	D10	Data bit 10.
41	37	D11	Data bit 11 (MSB).
42	38	AV_{CC}	Analog positive power supply, +5V.
43	39	OVF	Overflow output. Active high when either an overrange or underrange analog input condition is detected.
44	40	IRQ	Interrupt ReQuest output. Goes low when a conversion is complete.

Detailed Description

The HI5800 is a 12-bit two step sampling analog to digital converter which uses a subranging technique with digital error correction. As illustrated in the block diagram, it uses a sample and hold front end, 7-bit R-2R D/A converter which is laser trimmed to 14 bits accuracy, a 7-bit BiCMOS flash converter, precision bandgap reference, digital controller and timing generator, error correction logic, output latches and BiCMOS output drivers.

The falling edge of the convert command signal puts the sample and hold (S/H) in the hold mode and the conversion process begins. At this point the Interrupt Request (IRQ) line is set high indicating that a conversion is in progress. The output of the S/H circuit drives the input of the 7-bit flash converter through a switch. After allowing the flash to settle, the intermediate output of the flash is stored in the latches which feed the D/A and error correction logic. The D/A reconstructs the analog signal and feeds the gain amplifier whose summing node subtracts the held signal of the S/H and amplifies the residue by 32. This signal is then switched to the flash for a second pass using the input switch. The output of the second flash conversion is fed directly to the error correction which reconstructs the twelve bit word from the fourteen bit input. The logic also decodes the overflow bit and the polarity of the overflow. The output of the error correction is then gated through the read controller to the output drivers. The data is ready on the bus as soon as the IRQ line goes low.

I/O Control Inputs

The converter has four active low inputs ($\overline{CS}$, $\overline{CONV}$, $\overline{OE}$ and $\overline{A0}$) and fourteen outputs (D0-D11, IRQ and OVF). All inputs and outputs are TTL compatible and will also interface to the newer TTL compatible families. All four inputs are CMOS high input impedance stages and all outputs are BiMOS drivers capable of driving 100pF loads.

In order to initiate a conversion or read the data bus, $\overline{CS}$ should be held low. The conversion is initiated by the falling edge of the $\overline{CONV}$ command. The $\overline{OE}$ input controls the output bus directly and is independent of the conversion process. The data on the bus changes just before the IRQ goes low. Therefore if the $\overline{OE}$ line is held low all the time, the data on the bus will change just before the IRQ line goes low. The byte control signal $\overline{A0}$ is also independent of the conversion process and the byte can be manipulated anytime. When $\overline{A0}$ is low the 12 bits and overflow word is read on the bus. The bus can also be hooked up such that the upper byte (D11 to D4) is read when $\overline{A0}$ is low. When $\overline{A0}$ is high, the lower byte (D3 to D0) is output on the same eight pins with trailing zeros.

In order to minimize switching noise during a conversion, byte manipulations done using the $\overline{A0}$ signal should be done in the single shot mode and $\overline{A0}$ should be changed during the acquisition phase. For accuracy, allow sufficient time for settling from any glitches before the next conversion.

Once a conversion is started, the converter will complete the conversion and acquisition periods irrespective of the input states. If during these cycles another convert command is issued, it will be ignored until the acquire phase is complete.

Stand Alone Operation

The converter can be operated in a stand alone configuration with bus inputs controlling the converter. The conversion will be started on the negative edge of the convert ($\overline{CONV}$) pulse as long as this pulse is less than the converter throughput rate. If the converter is given multiple convert commands, it will ignore all but the first command until such time when the acquisition period of the next cycle is complete. At this point it will start a new conversion on the first negative edge of the input command. This allows the converter to be synchronized to a multiple of a faster external clock. The new output data of the conversion is available on the same cycle at the negative edge of the IRQ pulse and is valid until the next negative edge of the IRQ pulse. Data may be accessed at any time during these cycles. It should be noted that if the data bus is kept enabled all the time ($\overline{OE}$ is low), then the data will be updating just before the IRQ goes low. During this time, the data may not be valid for a few nanoseconds.

Continuous Convert Mode

The converter can be operated at its maximum rate by taking the $\overline{CONV}$ line low (supplying the first negative edge) and holding it low. This enables the continuous convert mode. During this time, at the end of the internal acquisition period, the converter automatically starts a new conversion. The data will be valid between the IRQ negative edges.

Note that there is no pipeline delay on the data. The output data is available during the same cycle as the conversion and is valid until the next conversion ends. This allows data access to both previous and present conversions in the same cycle.

When initiating a conversion or a series of conversions, the last signal ($\overline{CS}$ and $\overline{CONV}$) to arrive dominates the function. The same condition holds true for enabling the bus to read the data ($\overline{CS}$ and $\overline{OE}$). To terminate the bus operations, the first signal ($\overline{CS}$ and $\overline{OE}$) to arrive dominates the function.

Interrupt Request Output

The interrupt request line (IRQ) goes high at the start of each conversion and goes low to indicated the start of the acquisition. During the time that IRQ is high, the internal sample and hold is in hold mode. At the termination of IRQ, the sample and hold switches to acquire mode which lasts approximately 100ns. If no convert command is issued for a period of time, the sample and hold simply remains in acquire mode tracking the analog input signal until the next conversion cycle is initiated. The IRQ line is the only output that is not tristateable.

Analog Input, V_{IN}

The analog input of the HI5800 is coupled into the input stage of the Sample and Hold amplifier. The input is a high impedance bipolar differential pair complete with an ESD protection circuit. Typically it has >10MΩ input impedance. With this high input impedance circuit, the HI5800 is easily interfaced to any type of op-amp without a requirement for a

high drive capability. Adequate precautions should be taken while driving the input from high voltage output op-amps to ensure that the analog input pin is not overdriven above the specified maximum limits. For a +2.5V reference, the analog input range is ±2.5V. This input range scales with the value of the external reference voltage if the internal reference is not used. For best performance, the analog ground pin next to the analog input should be utilized for signal return.

Voltage Reference, REF_{OUT}

The HI5800 has a curvature corrected internal band-gap reference generator with a buffer amplifier capable of driving up to 15mA. The band-gap and amplifier are trimmed to give +2.50V. When connected to the reference input pin REF_{IN}, the reference is capable of driving up to 2mA externally. Further loading may degrade the performance of the output voltage. It is recommended that the output of the reference be decoupled with good quality capacitors to reduce the high-frequency noise.

Reference Input, REF_{IN}

The converter requires a voltage reference connected to the REF_{IN} pin. This can be the above internal reference or it can be an external reference. The REF_{IN} pin is approximately 200Ω input impedance and care should be taken to ensure that the external reference is capable of driving this input impedance. It is also recommended that adequate high frequency decoupling is provided at the reference input pin in order to minimize overall converter noise.

Error Adjustments

For most applications the accuracy of the HI5800 is sufficient without any adjustments. In applications where accuracy is of utmost importance three external adjustments are possible: S/H offset, D/A offset and D/A gain. Figure 4 illustrates the use of external potentiometers to reduce the HI5800 errors to zero.

The D/A offset (RO_{ADJ}) and S/H offset (ADJ+ and ADJ-) trims adjust the voltage offset of the transfer curve while the D/A gain trim (RG_{ADJ}) adjusts the tilt of the transfer curve around the curve midpoint (code 2048). The 10KΩ potentiometers can be installed to achieve the desired adjustment in the following manner.

Typically only one of the offset trimpots needs to be used. The offset should first be adjusted to get code 2048 centered at a desired DC input voltage such as zero volts. Next the gain trim can be adjusted by trimming the gain pot until the 4094 to 4095 code transition occurs at the desired voltage (2.500 - 1.5LSBs for a 2.5V reference). The gain trim can also be done by adjusting the gain pot until the code 0 to 1 transition occurs at a particular voltage (-2.5 + 0.5LSBs for a 2.5V reference). If a nonzero offset is needed, then the offset pot can be adjusted after the gain trim is finished. The gain trim is simplified if an offset trim to zero is done first with a nonzero offset trim done after the gain trim is finished. The D/A offset and S/H offset trimpots have an identical effect on the converter except that the S/H offset is a finer resolution trim. The D/A offset and D/A gain typically have an adjustment range of ±30LSBs and the S/H offset typically has an adjustment range of ±20LSBs.

If no external adjustments are required the following pins should be connected to analog ground (AGND) for optimum performance: RO_{ADJ}, RG_{ADJ}, ADJ+, and ADJ-.

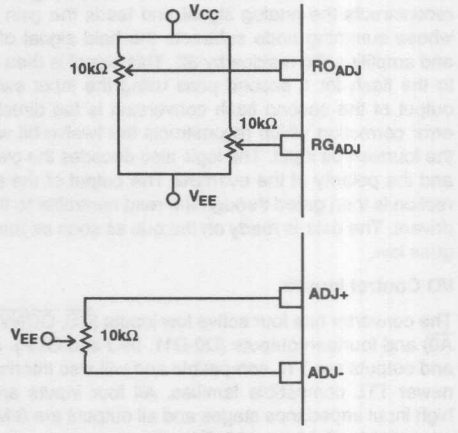


FIGURE 4. D/A OFFSET, D/A GAIN AND S/H OFFSET ADJUSTMENTS.

Typical Application Schematic

Figure 5 shows a typical schematic diagram for the HI5800. The adjust pins are shown with 10KΩ potentiometers used for gain and offset adjustments. These potentiometers may be left out and the respective pins should be connected to ground for best untrimmed performance.

TABLE 2. I/O TRUTH TABLE

INPUTS				OUTPUT	
$\overline{CS}$	$\overline{CONV}$	$\overline{OE}$	$\overline{A0}$	IRQ	FUNCTION
1	X	X	X	X	No operation.
0	0	X	X	X	Continuous convert mode.
0	X	0	0	X	Outputs all 12-bits and OVF or upper byte D11-D4 in 8 bit mode.
0	X	0	1	X	In 8 bit mode, outputs lower LSBs D3-D0 followed by 4 trailing zeroes and OVF, (See text).
0	1	X	X	0	Converter is in acquisition mode.
0	X	X	X	1	Converter is busy doing a conversion.
0	X	1	X	X	Data outputs and OVF in high impedance state.

X's = Don't Care

TABLE 3. A/D OUTPUT CODE TABLE

CODE DESCRIPTION LSB = $\frac{2(REF_{IN})}{4096}$	INPUT VOLTAGE* REF_{IN} = 2.5V (V)	OUTPUT DATA (OFFSET BINARY) MSB												LSB
		OVF	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
≥+FS	≥ +2.5000	1	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1LSB	+2.49878	0	1	1	1	1	1	1	1	1	1	1	1	1
+3/4FS	+1.8750	0	1	1	1	0	0	0	0	0	0	0	0	0
+1/2FS	+1.2500	0	1	1	0	0	0	0	0	0	0	0	0	0
+1LSB	+0.00122	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	1	0	0	0	0	0	0	0	0	0	0	0
-1 LSB	-0.00122	0	0	1	1	1	1	1	1	1	1	1	1	1
-1/2FS	-1.2500	0	0	1	0	0	0	0	0	0	0	0	0	0
-3/4FS	-1.8750	0	0	0	1	0	0	0	0	0	0	0	0	0
-FS + 1LSB	-2.49878	0	0	0	0	0	0	0	0	0	0	0	0	1
≤-FS	≤ -2.5000	1	0	0	0	0	0	0	0	0	0	0	0	0

* The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.

Definitions

Static Performance Definitions

Offset, fullscale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus fullscale values. The results are all displayed in LSB's.

Offset Error (VOS)

The first code transition should occur at a level 1/2LSB above the negative fullscale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Fullscale Error (FSE)

The last code transition should occur for a analog input that is 1 and 1/2 LSB's below positive fullscale. Fullscale error is defined as the deviation of the actual code transition from this point.

Gain Error

Gain error is calculated by dividing the measured fullscale range by the ideal fullscale range. Note that this is adjustable to zero.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1LSB. The converter is guaranteed for no missing codes over all temperature ranges.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error is noted. The number reported is the percent change in these parameters versus fullscale divided by the percent change in the supply.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5800. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The data is taken with a coherent test system to avoid all the inaccuracies of having to use window functions. The sine wave input to the part is -0.5db down from fullscale for all these tests. All results are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured rms signal to rms noise at a specified input and sampling frequency. The noise is the rms sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured rms signal to rms sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first 5 harmonic components to the rms value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental rms amplitude to the rms amplitude of the next largest spur or spectral component If the harmonics are buried in the noise floor it is the largest peak.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f1 and f2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The IMD products used to calculate the total distortion are (f2-f1), (f2+f1), (2f1-f2), (2f1+f2), (2f2-f1), (2f2+f1), (3f1-f2), (3f1+f2), (3f2-f1), (3f2+f1), (2f2-2f1), (2f2+2f1), (2f1), (2f2), (2f1), (2f2), (4f1), (4f2). The data reflects the sum of all the IMD products.

HARRIS SEMICONDUCTOR

HI5801

ADVANCE INFORMATION

July 1992

12-Bit, 5MSPS A/D Converter

Features

- 200ns Conversion Time
- 12-Bit No Missing Codes Over Temperature
- 0.5LSB DNL/1.0LSB INL
- High Input Bandwidth
- Precision Voltage Reference
- ± 2.5V Input Signal Range
- Zero Latency/No Pipeline Delay

Applications

- High Speed Data Acquisition Systems
- Medical Imaging
- Radar Signal Analysis
- Document and Film Scanners
- Vibration/Waveform Spectrum Analysis
- Digital Servo Control

Description

The HI5801 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in the HBC10 BiCMOS process. It is a complete subsystem containing voltage reference, two-step subranging A/D, error correction, control logic, and timing generator. The HI5801 is designed for high speed applications where wide bandwidth, accuracy and low distortion are essential.

The HI5801 is available in Commercial and Industrial temperature ranges and is offered in a 40 pin ceramic DIP and a 44 pin PLCC package.

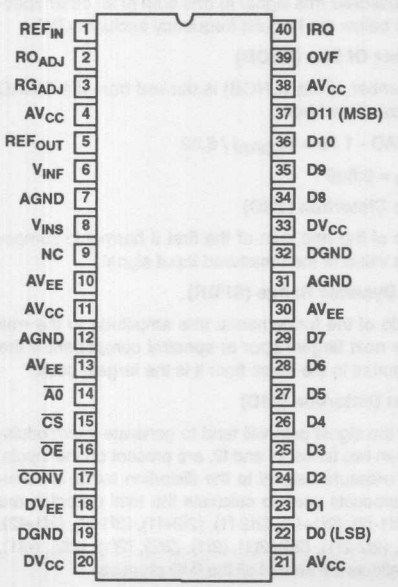
Ordering Information

PART NUMBER	LINEARITY	TEMP. RANGE	PACKAGE
HI5801AIJ	±2LSB	-40°C to +85°C	40 Pin CERDIP
HI5801BIJ	±1LSB	-40°C to +85°C	40 Pin CERDIP
HI5801JCM*	±2LSB	0°C to +75°C	44 Pin PLCC
HI5801KCM*	±1LSB	0°C to +75°C	44 Pin PLCC

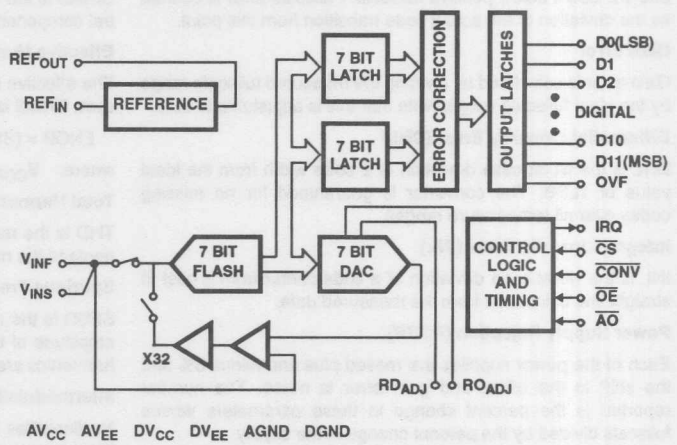
* Consult Factory for Availability

Pinout

40 PIN CERDIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3287

HARRIS SEMICONDUCTOR

HI5812

CMOS 12-Bit Sampling A/D Converter with Internal Track and Hold

July 1992

Features

- 20µs Conversion Time
- 50KSPS Throughput Rate
- Built-In Track and Hold
- Guaranteed No Missing Codes Over Temperature
- Single +5V Supply Voltage
- 25mW Maximum Power Consumption
- Internal or External Clock

Applications

- Remote Low Power Data Acquisition Systems
- Digital Audio
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement Systems

Description

The HI5812 is a fast, low power, 12-bit successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 1.9mA when operating at 5V. The HI5812 features a built-in track and hold. The conversion time is as low as 15µs with a 5V supply.

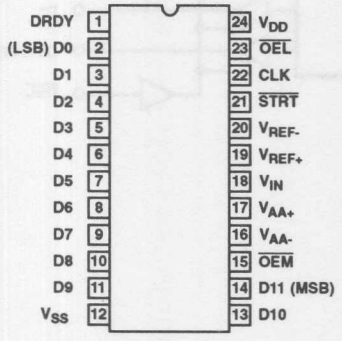
The twelve data outputs feature full high speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.) 12-bit, 8-bit (MSB's), and/or 4-bit (LSB's). A data ready flag, and conversion-start inputs complete the digital interface.

An internal clock is provided and is available as an output. The clock may also be over-driven by an external source.

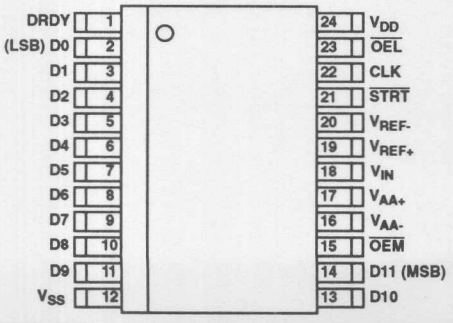
The HI5812 is rated over the full industrial temperature range and is offered in 24 lead narrow body Plastic Dip, narrow body CERDIP, and wide body Plastic SOIC packages.

Pinouts

NARROW PLASTIC DIP AND CERDIP
TOP VIEW



WIDE PLASTIC SOIC
TOP VIEW



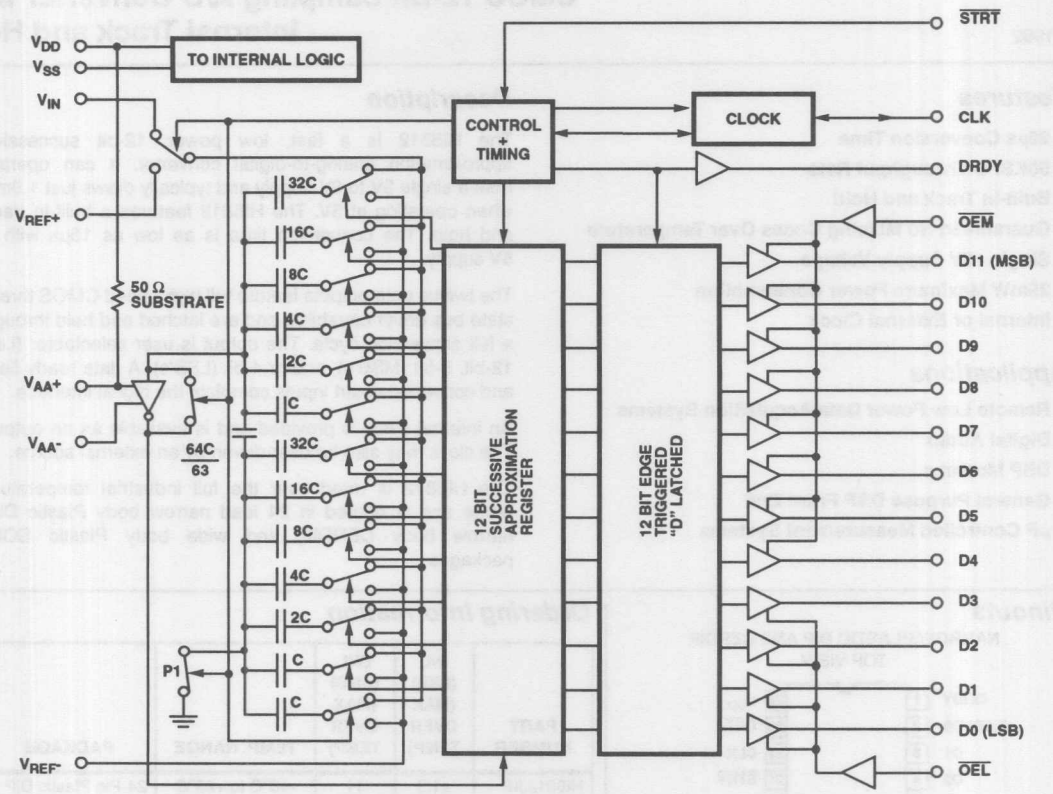
Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP)	DNL (BITS) (MAX OVER TEMP)	TEMP. RANGE	PACKAGE
HI5812JIP	±1.5	11	-40°C to +85°C	24-Pin Plastic DIP
HI5812KIP	±1.0	12	-40°C to +85°C	24-Pin Plastic DIP
HI5812JIB	±1.5	11	-40°C to +85°C	24-Pin Plastic SOIC
HI5812KIB	±1.0	12	-40°C to +85°C	24-Pin Plastic SOIC
HI5812JIJ	±1.5	11	-40°C to +85°C	24-Pin CERDIP
HI5812KIJ	±1.0	12	-40°C to +85°C	24-Pin CERDIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3214.1**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} ..... (V_{SS} -0.5 V) < V_{DD} < +6.5 V
- V_{AA}+ to V_{AA}- ..... (V_{SS} -0.5 V) to (V_{SS} +6.5 V)
- V_{AA}+ to V_{DD} ..... ±0.3 V

Analog and Reference Inputs
- V_{IN}, V_{REF+}, V_{REF-} ..... (V_{SS} -0.3 V) < V_{INA} < (V_{DD} +0.3 V)

Digital I/O Pins ..... (V_{SS} -0.3 V) < VI/O < (V_{DD} +0.3 V)

Operating Temperature Range
- Plastic DIP, Plastic SOIC, and CERDIP ..... -40°C to +85°C

Junction Temperature
- Plastic Dip and Plastic SOIC ..... +150°C
- CERDIP ..... +175°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... 300°C

Thermal Information

Thermal Resistance	θja	θjc
Plastic DIP	51°C/W	21°C/W
Plastic SOIC	75°C/W	23°C/W
CERDIP	50°C/W	11°C/W

Power Dissipation at +75°C (Note 1)
- Plastic DIP ..... 1.5 W
- Plastic SOIC ..... 1.0 W
- CERDIP ..... 2.0 W

Power Dissipation Derating Factor above +75° C
- Plastic DIP ..... 20 mW/°C
- Plastic SOIC ..... 13 mW/°C
- CERDIP ..... 20 mW/°C

NOTE: 1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = V_{AA+} = 5V, V_{REF+} = +4.608V, V_{SS} = V_{AA-} = V_{REF-} = GND, CLK = External 750kHz, Unless Otherwise Noted.

PARAMETER		TEST CONDITION	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS -40°C to +85°C MIN	LIMITS -40°C to +85°C MAX	UNITS
ACCURACY								
Resolution			12			12		Bits
Integral Linearity Error, INL (End Point)	J				±1.5		±1.5	LSB
	K				±1.0		±1.0	LSB
Differential Linearity Error, DNL No Missing Codes	J		11			11		Bits
	K		12			12		Bits
Gain Error, FSE (Adjustable to Zero)	J				±3.0		±3.0	LSB
	K				±2.5		±2.5	LSB
Offset Error, VOS (Adjustable to Zero)	J				±2.0		±2.0	LSB
	K				±1.0		±1.0	LSB
Power Supply Rejection, PSRR		V_{REF} = 4V						
Offset Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		0.1	±0.5		±0.5	LSB
Gain Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		0.1	±0.5		±0.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD = RMS Signal / RMS Noise + Distortion	J	f_S = Internal Clock, f_{IN} = 1kHz		68.8				dB
		f_S = 750kHz, f_{IN} = 1kHz		69.2				dB
	K	f_S = Internal Clock, f_{IN} = 1kHz		71.0				dB
		f_S = 750kHz, f_{IN} = 1kHz		71.5				dB
Signal to Noise Ratio, SNR = RMS Signal / RMS Noise	J	f_S = Internal Clock, f_{IN} = 1kHz		70.5				dB
		f_S = 750kHz, f_{IN} = 1kHz		71.1				dB
	K	f_S = Internal Clock, f_{IN} = 1kHz		71.5				dB
		f_S = 750kHz, f_{IN} = 1kHz		72.1				dB

Electrical Specifications $V_{DD} = V_{AA+} = 5V$, $V_{REF+} = +4.608V$, $V_{SS} = V_{AA-} = V_{REF-} = GND$, CLK = External 750kHz, Unless Otherwise Noted. **(Continued)**

PARAMETER		TEST CONDITION	LIMITS +25°C MIN	+25°C TYP	+25°C MAX	-40°C to +85°C MIN	-40°C to +85°C MAX	UNITS
Total Harmonic Distortion, THD	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz		-73.9 -73.8				dBc dBc
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz		-80.3 -79.0				dBc dBc
Spurious Free Dynamic Range, SFDR	J	f_S =Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz		-75.4 -75.1				dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz		-80.9 -79.6				dB dB
ANALOG INPUT								
Input Current, Dynamic		At $V_{IN} = V_{REF}+$, 0V		±50	±100		±100	µA
Input Current, Static		Conversion Stopped		±0.4	±10		±10	µA
Input Bandwidth -3dB				1				MHz
Reference Input Current				160				µA
Input Series Resistance, R_S		In Series with Input C_{SAMPLE}		420				Ω
Input Capacitance, C_{SAMPLE}		During Sample State		380				pF
Input Capacitance, C_{HOLD}		During Hold State		20				pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$								
High-Level Input Voltage, V_{IH}			2.4			2.4		V
Low-Level Input Voltage, V_{IL}					0.8		0.8	V
Input Leakage Current, I_{IL}		Except CLK, V_{IN} = 0V, 5V			±10		±10	µA
Input Capacitance, C_{IN}				10				pF
DIGITAL OUTPUTS								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -400µA	4.6			4.6		V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 1.6mA			0.4		0.4	V
Three-state Leakage, I_{OZ}		Except DRDY, V_{OUT}= 0V, 5V			±10		±10	µA
Output Capacitance, C_{OUT}		Except DRDY		20				pF
CLOCK								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -100µA (Note 2)	4			4		V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 100µA (Note 2)			1		1	V
Input Current		CLK Only, V_{IN} = 0V, 5V			±5		±5	mA

Electrical Specifications $V_{DD} = V_{AA+} = 5V$, $V_{REF+} = +4.608V$, $V_{SS} = V_{AA-} = V_{REF-} = GND$, CLK = External 750kHz, Unless Otherwise Noted. **(Continued)**

PARAMETER	TEST CONDITION	LIMITS					UNITS
		+25°C			-40°C to +85°C		
		MIN	TYP	MAX	MIN	MAX	
TIMING							
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time)		20			20		µs
Clock Frequency	Internal Clock, (CLK = Open)	200	300	400	150	500	kHz
	External CLK (Note 2)	0.05	2	1.5	0.05	1.5	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	External CLK (Note 2)	100			100		ns
Aperture Delay, t_DAPR	(Note 2)		35	50		70	ns
Clock to Data Ready Delay, t_{D1}DRDY	(Note 2)		105	150		180	ns
Clock to Data Ready Delay, t_{D2}DRDY	(Note 2)		100	160		195	ns
Clock to Data Ready, t_DDATA	(Note 2)		75	110		135	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	0	-75		0		ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60		100		ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	10	4		15		ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)		65	105		120	ns
Clock Delay from Start, $t_D\overline{STRT}$	(Note 2)		60				ns
Output Enable Delay, t_{EN}	(Note 2)		20	30		50	ns
Output Disabled Delay, t_{DIS}	(Note 2)		80	95		120	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$			1.9	5		8	mA

NOTE:

2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams

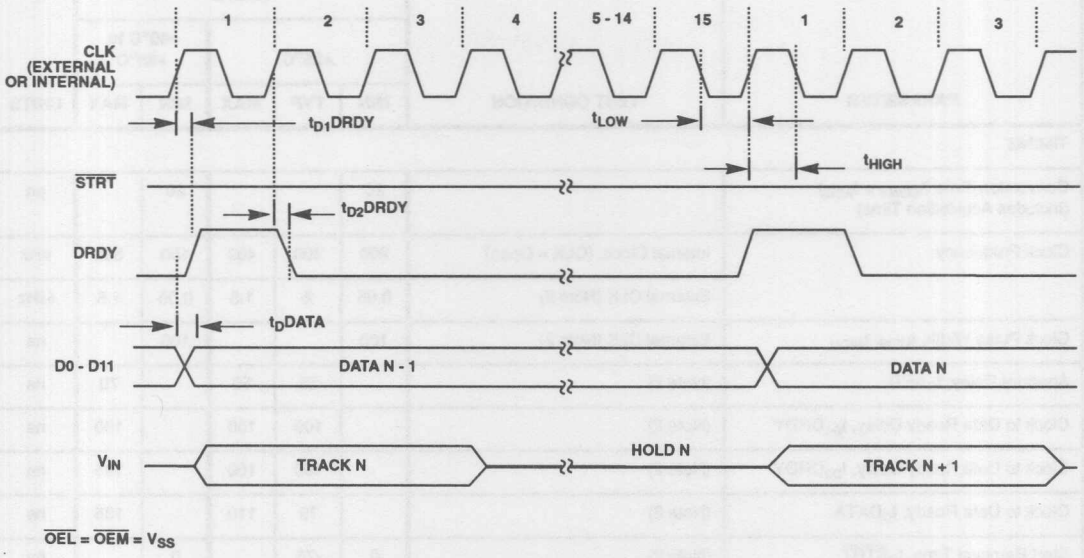


FIGURE 1. CONTINUOUS CONVERSION MODE

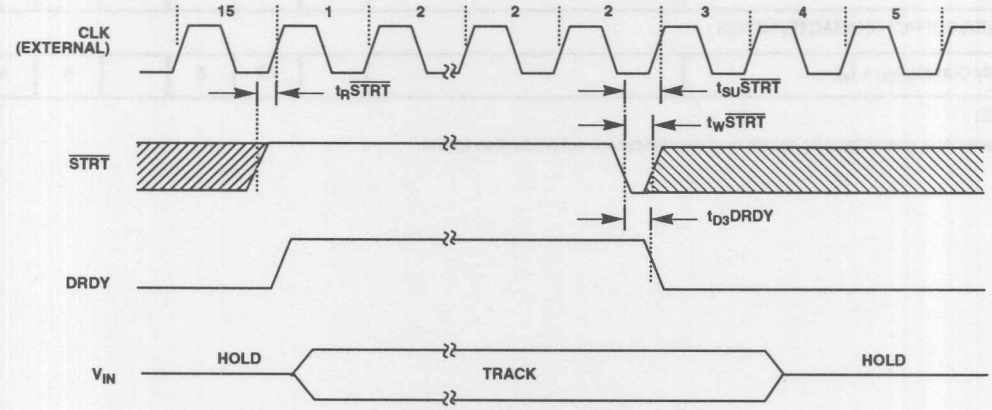


FIGURE 2. SINGLE SHOT MODE EXTERNAL CLOCK

Timing Diagrams (Continued)

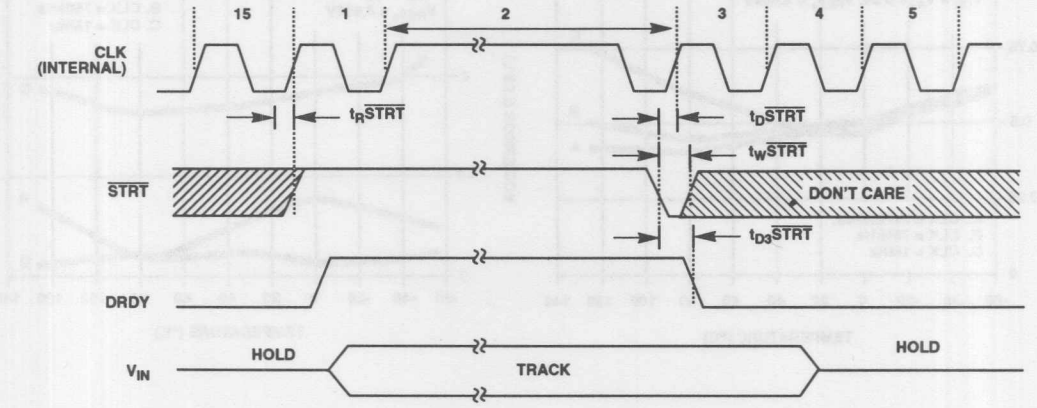


FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK

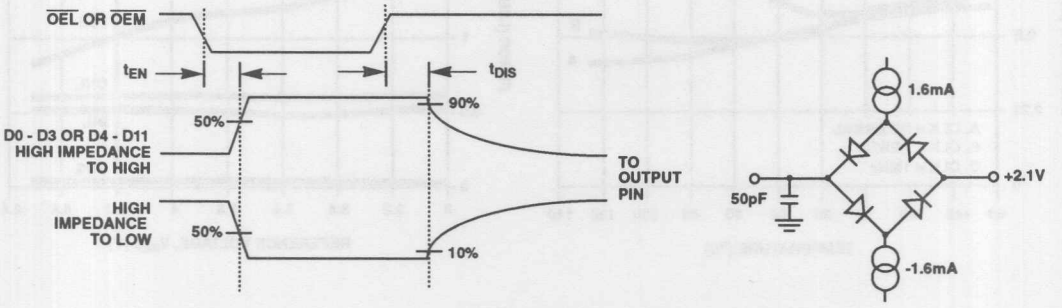


FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

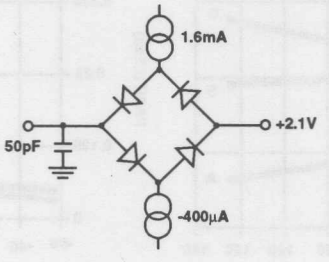
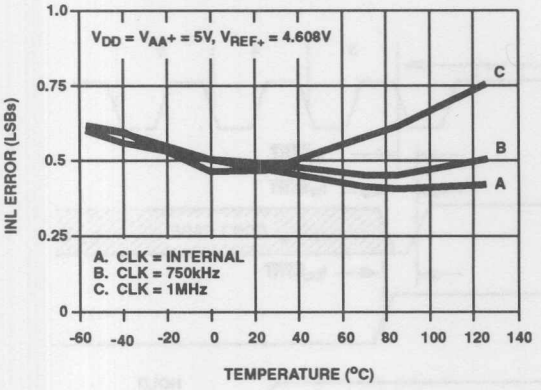


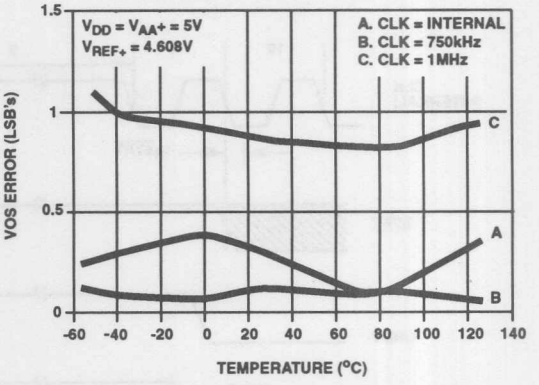
FIGURE 5. GENERAL TIMING LOAD CIRCUIT

Typical Performance Curves

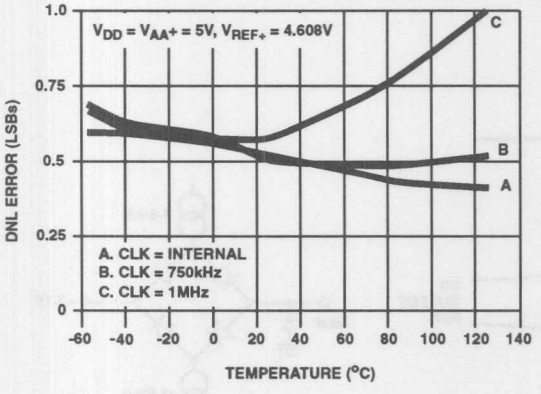
INL vs TEMPERATURE



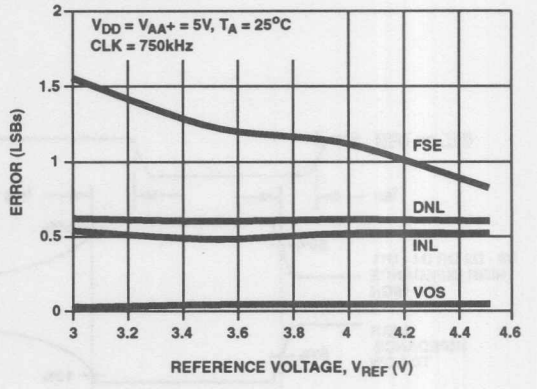
OFFSET VOLTAGE vs TEMPERATURE



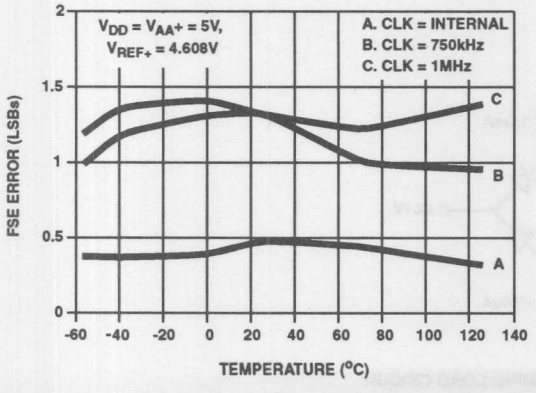
DNL vs TEMPERATURE



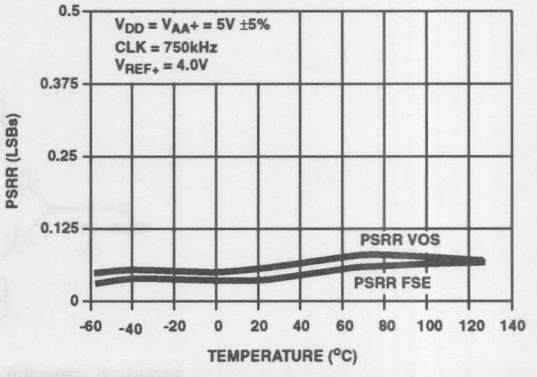
ACCURACY vs REFERENCE VOLTAGE



FULL SCALE ERROR vs TEMPERATURE

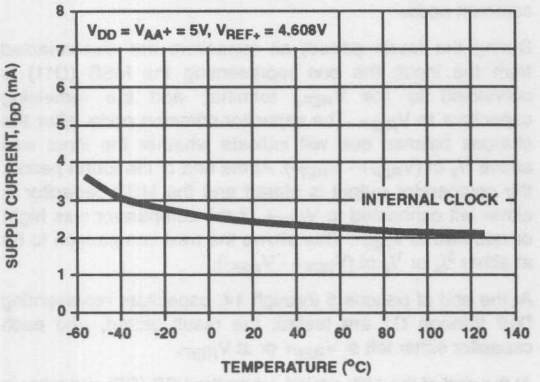


POWER SUPPLY REJECTION vs TEMPERATURE

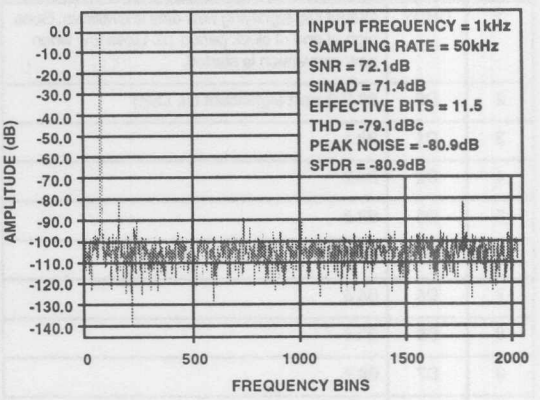


Typical Performance Curves

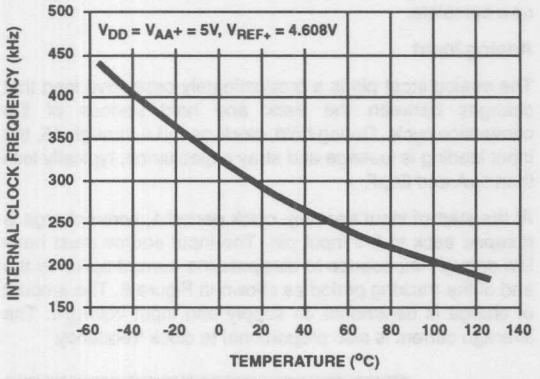
SUPPLY CURRENT vs TEMPERATURE



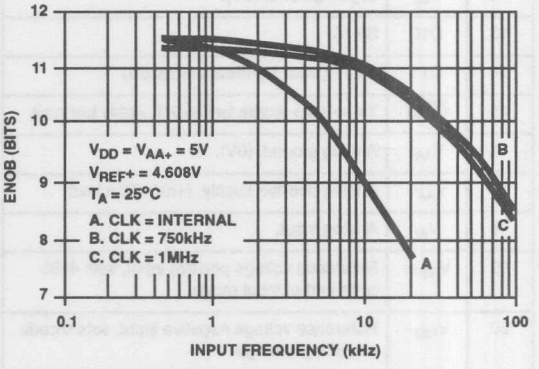
FFT SPECTRUM



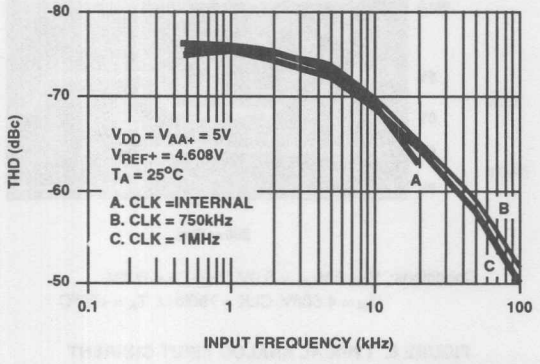
INTERNAL CLOCK FREQUENCY vs TEMPERATURE



EFFECTIVE BITS vs INPUT FREQUENCY



TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY



SIGNAL-NOISE RATIO vs INPUT FREQUENCY

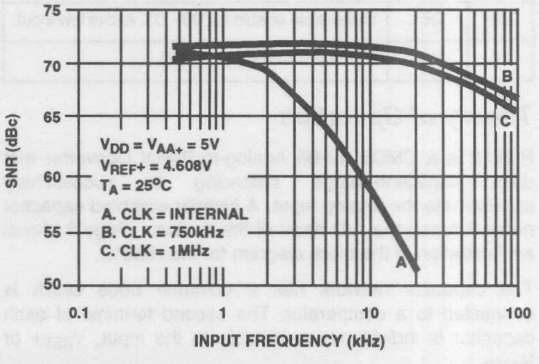


TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit 0 (Least significant bit, LSB)
3	D1	Bit 1
4	D2	Bit 2
5	D3	Bit 3
6	D4	Bit 4
7	D5	Bit 5
8	D6	Bit 6
9	D7	Bit 7
10	D8	Bit 8
11	D9	Bit 9
12	V_{SS}	Digital ground, (0V).
13	D10	Bit 10
14	D11	Bit 11 (Most significant bit, MSB)
15	$\overline{OEM}$	Three-state enable for D4-D11. Active low input.
16	V_{AA}-	Analog ground, (0V).
17	V_{AA}+	Analog positive supply. (+5V) (See text)
18	V_{IN}	Analog input.
19	V_{REF}+	Reference voltage positive input, sets 4095 code end of input range.
20	V_{REF}-	Reference voltage negative input, sets 0 code end of input range.
21	$\overline{STRT}$	Start conversion input active low, recognized after end of clock period 15.
22	CLK	CLK input or output. Conversion functions are synchronized to positive going edge. (See text)
23	$\overline{OEL}$	Three-state enable for D0 - D3. Active low input.
24	V_{DD}	Digital positive supply (+5V).

Theory of Operation

HI5812 is a CMOS 12-Bit Analog-to-Digital Converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the A/D heart of the device. Page 2 shows an illustration of the block diagram for the HI5812.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}+ or V_{REF}-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto-balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the V_{REF+} terminal; and the remaining capacitors to V_{REF}-. The capacitor-common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of (V_{REF}+ - V_{REF}-). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}+ (if the comparator was high) or returned to V_{REF}-. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of (V_{REF}+ - V_{REF}-).

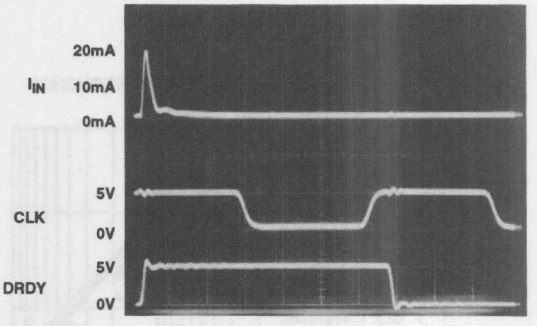
At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at V_{REF}+ or at V_{REF}-.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 6. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.



Conditions: $V_{DD} = V_{AA+} = 5.0V$, $V_{REF+} = 4.608V$, $V_{IN} = 4.608V$, CLK = 750kHz, $T_A = +25°C$

FIGURE 6. TYPICAL ANALOG INPUT CURRENT

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With an external clock of 750kHz the track period is 4µs.

A simplified analog input model is presented in Figure 7. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 4µs acquisition time settling to within 0.5LSB is 750Ω.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.

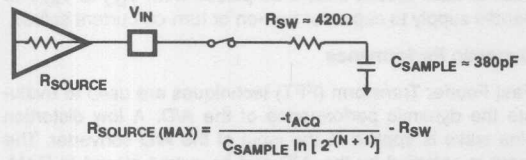
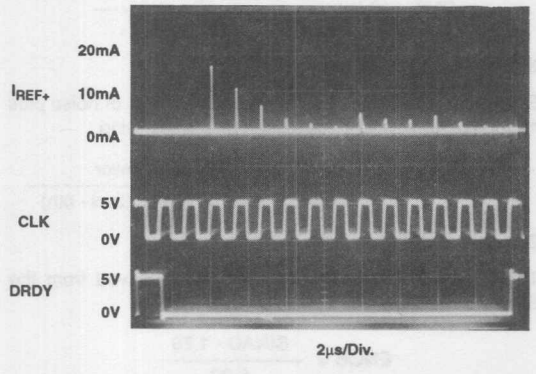


FIGURE 7. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

As shown in Figure 8, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge-balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.



Conditions: $V_{DD} = V_{AA+} = 5.0V$, $V_{REF+} = 4.608V$, $V_{IN} = 2.3V$, CLK = 750kHz, $T_A = +25°C$

FIGURE 8. TYPICAL REFERENCE INPUT CURRENT

The HI5812 is specified with a 4.608V reference, however, it will operate with a reference down to 3V having a slight degradation in performance. A typical graph of accuracy vs reference voltage is presented.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5812 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5812 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by T_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by T_{D1}DRDY) after the start of clock period 1, and returns low (specified by T_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on three-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). T_{EN} and T_{DIS} specify the output enable and disable times.

If the output data is to be latched externally by the DRDY signal, the trailing edge of DRDY should be used: there is no guaranteed setup time.

When $\overline{STRT}$ input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the $\overline{STRT}$ signal is removed (at least $T_R\overline{STRT}$) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

A low signal applied to $\overline{STRT}$ (at least $T_W\overline{STRT}$ wide) can now initiate a new conversion. The $\overline{STRT}$ signal (after a delay of (T_DCLK) cause the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external clock. If $\overline{STRT}$ is removed (at least $T_R\overline{STRT}$) before clock period 2, a low signal applied to $\overline{STRT}$ will drop the DRDY flag as before, and with the first positive-going clock edge that meets the ($T_{SU}\overline{STRT}$) setup time, the converter will continue with clock period 3.

Clock

The HI5812 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronized with the rising edge of the clock signal.

Figure 9 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.

The internal clock will shut down if the A/D is not restarted after a conversion. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minium frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge-pump voltage to decay.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum T_{LOW} and T_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

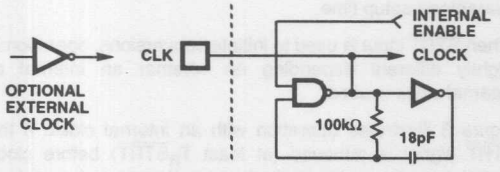


FIGURE 9. INTERNAL CLOCK CIRCUITRY

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{AA}+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The V_{AA}+ and V_{AA}- terminals supply the charge-balancing comparator only. Because the comparator is auto-balanced between conversions, it has good low-frequency supply rejection. It does not reject well at high frequencies however; V_{AA}- should be returned to a clean analog ground and V_{AA}+ should be RC decoupled from the digital supply as shown in Figure 10.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}+. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A 10µF capacitor from V_{AA}+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to V_{AA}+ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured rms signal to rms sum of noise at a specified input and sampling frequency. The noise is the rms sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76) dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured rms signal to rms sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the rms sum of the second through sixth harmonic components to the fundamental rms signal for a specified input and sampling frequency.

$$THD = 10 \log \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental rms amplitude to the rms amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 3. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* V_{REF+} = 4.608V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	4.6069	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	4.6058	4094	1	1	1	1	1	1	1	1	1	1	1	0
3/4 FS	3.4560	3072	1	1	0	0	0	0	0	0	0	0	0	0
1/2 FS	2.3040	2048	1	0	0	0	0	0	0	0	0	0	0	0
1/4 FS	1.1520	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.001125	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

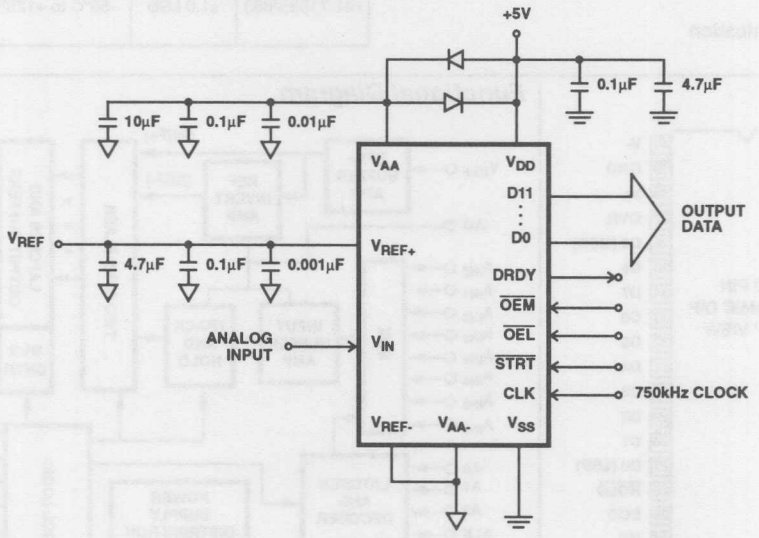


FIGURE 10. GROUND AND SUPPLY DECOUPLING

HARRIS SEMICONDUCTOR

HI-7153/883

8-Channel, 10-Bit, High Speed Sampling A/D Converter

July 1992

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **5μs Conversion Time**
- **8-Channel Input Multiplexer**
- **200,000 Channels/Second Throughput Rate**
- **Over 9 Effective Bits at 20kHz**
- **No Offset or Gain Adjustments Necessary**
- **Analog and Reference Inputs Fully Buffered**
- **On-Chip Track and Hold Amplifier**
- **μP Compatible Interface, 2's Complement Data Output**
- **150mW Power Consumption**
- **Single 2.5V Reference Required for a ±2.5V Input Range**
- **Out-of-Range Flag**

Applications

- **μP Controlled Data Acquisition Systems**
- **DSP**
  - **Avionics**
  - **Sonic**
- **Process Control**
- **Automotive Transducer Sensing**
  - **Industrial**
- **Robotics**
- **Digital Communication**

Description

The HI-7153/883 is an 8-channel high speed 10 bit A/D converter which uses a Two Step Flash algorithm to achieve throughput rates of 200kHz. The converter features an 8-channel CMOS analog multiplexer with random channel addressing. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

Internal high speed CMOS buffers at both the analog and reference inputs simplifies interface requirements.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor which reduces external circuitry.

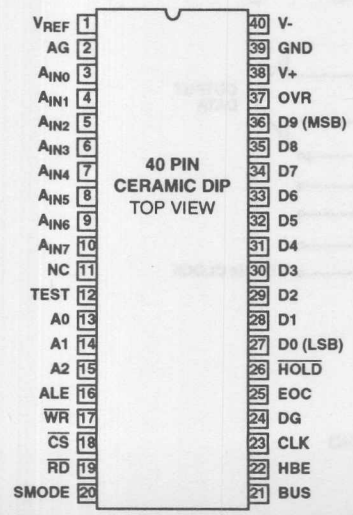
Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read and Write control signals. The digital three-state outputs are byte organized for bus interface to 8 to 16 bit systems. An Out-of-Range pin, together with the MSB bit, can be used to indicate an under or over-range condition.

The HI-7153/883 operates with ± 5V supplies. Only a single +2.5V reference is required to provide a bipolar input range from -2.5V to +2.5V.

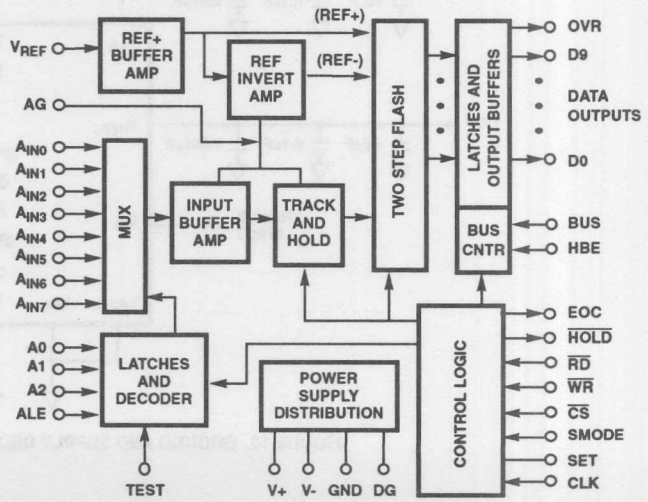
Ordering Information

PART NUMBER	LINEARITY (MAX ILE)	TEMPERATURE RANGE	PACKAGE
HI1-7153S/883	±1.0 LSB	-55°C to +125°C	40 Pin Ceramic DIP

Pinout



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3285**

Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	V_{REF}	Reference voltage input (+2.5V).
2	AG	Analog ground reference (0V).
3	A_{IN0}	Analog input channel 0.
4	A_{IN1}	Analog input channel 1.
5	A_{IN2}	Analog input channel 2.
6	A_{IN3}	Analog input channel 3.
7	A_{IN4}	Analog input channel 4.
8	A_{IN5}	Analog input channel 5.
9	A_{IN6}	Analog input channel 6.
10	A_{IN7}	Analog input channel 7.
11	NC	No connect or tie to V+ only.
12	TEST	Test pin. Connect to DG for normal operation.
13	A0	Mux address input. (LSB) Active high.
14	A1	Mux address input. Active high.
15	A2	Mux address input. (MSB) Active high.
16	ALE	Mux address enable. When high, the latch is transparent. Address data is latched on the falling edge.
17	$\overline{WR}$	Write input. With $\overline{CS}$ low, starts conversion when pulsed low; continuous conversions when kept low.
18	$\overline{CS}$	Chip select input. Active low
19	$\overline{RD}$	Read input. With $\overline{CS}$ low, enable output buffers when pulsed low; outputs updated at the end of conversion.
20	SMODE	Slow memory mode input. Active high.
21	BUS	Bus select input. HIgh = all inputs enabled together D0 - D9, OVR Low = Outputs enabled by HBE.
22	HBE	Byte select (HBE/LBE) input for 8-bit bus. High = High byte selece, D0 - D7.
23	CLK	Clock input, TTL compatible.
24	DG	Digital ground (0V).

PIN #	SYMBOL	DESCRIPTION
25	EOC	End-of-conversion status. Pulses high at the end-of-conversion.
26	$\overline{HOLD}$	Start of conversion status. Pulses low at the start-of-conversion.
27	D0	Bit 0 (LSB).
28	D1	Bit 1.
29	D2	Bit 2 Output.
30	D3	Bit 3 Data.
31	D4	Bit 4 Bits.
32	D5	Bit 5.
33	D6	Bit 6.
34	D7	Bit 7.
35	D8	Bit 8.
36	D9	Bit 9 (MSB).
37	OVR	Out of Range flag. Valid at end of conversion when output exceeds full scale.
38	V+	Positive supply voltage input (+5V).
39	GND	Ground return for comparators (0V).
40	V-	Negative supply voltage input (-5V).

Multiplexer Channel Selection

ADDRESS & CONTROL INPUTS					ANALOG CHANNEL SELECTED
A2	A1	A0	$\overline{CS}$	ALE	
0	0	0	0	1	A_{IN0}
0	0	1	0	1	A_{IN1}
0	1	0	0	1	A_{IN2}
0	1	1	0	1	A_{IN3}
1	0	0	0	1	A_{IN4}
1	0	1	0	1	A_{IN5}
1	1	0	0	1	A_{IN6}
1	1	1	0	1	A_{IN7}

Truth Tables

SLOW MEMORY MODE I/O TRUTH TABLE (SMODE = V+)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Initiates a conversion.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 and OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR.
X	X	1	X	X	X	Disables all outputs (high impedance).

NOTE: X = don't care.

FAST MEMORY MODE I/O TRUTH TABLE (SMODE = DG)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Continuous conversion, $\overline{WR}$ may be tied to DG.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 and OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR.
X	X	1	X	X	X	Disables all outputs (high impedance).

NOTE: X = don't care.

DMA MODE I/O TRUTH TABLE (SMODE = V+, $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = DG))

BUS	HBE	ALE	FUNCTION
X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	Enables D0 - D9 and OVR.
0	0	X	Low byte enable: D0 - D7
0	1	X	High byte enable: D8 - D9, OVR.

NOTE: X = don't care.

Absolute Maximum Ratings

Supply Voltage
V+ to GND (DG/AG/GND) ..... -0.3V < V+ <+5.7V
V- to GND (DG/AG/GND) ..... -5.7V < V- <+0.3V
Analog and Reference Inputs
A_{IN0}-A_{IN7}, V_{REF} ..... (GND-0.3V) < V_{INA} < (V+ +0.3V)
Digital I/O Pins D0-D9, OVR, CLK, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ALE, SMODE, $\overline{HOLD}$, EOC, HBE, BUS, A0-A2, TEST (DG -0.3V) < V_{IO} < (V+ +0.3V)
Operating Temperature Range ..... -55°C to +125°C
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature, (Soldering 10 sec) ..... 300°C
ESD Classification ..... Class 1

Thermal Information

Thermal Resistance	θja	θjc
HI-7153/883	26°C/W	10°C/W

Power Dissipation at +75°C (Note 1)
HI-7153/883 ..... 3.9W
Power Dissipation Derating Factor Above +75°C
HI-7153/883 ..... 39mW/°C
Reliability Information
Transistor Count 1460
Worst Case Density ..... 2.5 x 10^4 A/cm^2

NOTE:
1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = 5V, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz with $t_R = t_F \leq 25$ns and 50% Duty Cycle, Unless Otherwise Specified.

SYMBOL	DC PARAMETER	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
ACCURACY							
ILE	Integral Linearity Error (Best Fit Line)		1	+25°C	-	±1.0	LSB
			2, 3	+125°C, -55°C	-	±1.0	LSB
DLE	Differential Linearity Error		1	+25°C	-	±1.0	LSB
			2, 3	+125°C, -55°C	-	±1.0	LSB
V_{OS}	Bipolar Offset Error		1	+25°C	-	±2.5	LSB
			2, 3	+125°C, -55°C	-	±3.0	LSB
FSE	Unadjusted Gain Error		1	+25°C	-	±2.5	LSB
			2, 3	+125°C, -55°C	-	±3.0	LSB
ANALOG MULTIPLEXER							
IBI	Input Leakage Current	A_{IN} = ±2.50V	1	+25°C	-	±100	nA
			2, 3	+125°C, -55°C	-	±100	nA
$R_{DS(ON)}$	MUX On-resistance	I_{IN} = 100µA	1	+25°C	-	2.5	KΩ
			2, 3	+125°C, -55°C	-	2.5	KΩ
REFERENCE INPUT							
IBR	Reference Input Bias Current	V_{REF} = +2.50V	1	+25°C	-	±100	nA
			2, 3	+125°C, -55°C	-	±100	nA
LOGIC INPUTS							
V_{IH}	Input High Voltage		1	+25°C	2.4	-	V
			2, 3	+125°C, -55°C	2.4	-	V
V_{IL}	Input Low Voltage		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
I_{IL}	Logic Input Current	V_{IN} = 0V, +5V	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±1	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V+ = 5V, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz with $t_R = t_F \leq 25$ns and 50% Duty Cycle, Unless Otherwise Specified.

SYMBOL	DC PARAMETER	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
LOGIC OUTPUTS							
V_{OH}	Output High Voltage	I_{OH} = -200µA	1	+25°C	2.4	-	V
			2, 3	+125°C, -55°C	2.4	-	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA	1	+25°C	-	0.4	V
			2, 3	+125°C, -55°C	-	0.4	V
I_{OL}	Output Leakage Current	$\overline{RD}$ = +5V, V_{OUT} = 5V, 0V (Note 11)	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±10	µA
POWER SUPPLY VOLTAGE RANGE							
V+	Positive Supply	Functional operation only. (Note 10)	7	+25°C	4.5	5.5	V
			8A, 8B	+125°C, -55°C	4.5	5.5	V
V-	Negative Supply	Functional operation only. (Note 10)	7	+25°C	-4.5	-5.5	V
			8A, 8B	+125°C, -55°C	-4.5	-5.5	V
POWER SUPPLY REJECTION							
FSE	V+, V- Gain Error	V+ = 5V, V- = -4.75V, -5.25V	1	+25°C	-	±0.5	LSB
			2, 3	+125°C, -55°C	-	±0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	1	+25°C	-	±0.5	LSB
			2, 3	+125°C, -55°C	-	±0.8	LSB
VOS	V+, V- Offset Error	V+ = 5V, V- = -4.75V, -5.25V	1	+25°C	-	±0.5	LSB
			2, 3	+125°C, -55°C	-	±0.8	LSB
		V- = 5V, V+ = 4.75V, 5.25V	1	+25°C	-	±0.5	LSB
			2, 3	+125°C, -55°C	-	±0.8	LSB
SUPPLY CURRENT							
I+	V+ Supply Current	V+ = 5V, V- = 5V	1	+25°C	-	30	mA
			2, 3	+125°C, -55°C	-	30	mA
I-	V- Supply Current	V+ = 5V, V- = 5V	1	+25°C	-	-15	mA
			2, 3	+125°C, -55°C	-	-15	mA

TABLE 2. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = 5V, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz with $t_R = t_F \leq 25$ns and 50% Duty Cycle, Unless Otherwise Specified.

SYMBOL	AC PARAMETERS	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
t_{SPS}	Continuous Conversion Time	(Note 3)	9	+25°C		5	µs
			10, 11	+125°C, -55°C		5	µs

TABLE 3. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V+ = 5V, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz with $t_R = t_F \leq 25$ns and 50% Duty Cycle, Unless Otherwise Specified.

SYMBOL	PARAMETER	NOTES	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
t_{SPS}	Continuous Conversion Time	3, 5	+25°C	60	5	µs
			+125°C, -55°C	60	5	µs
t_{CONV}	Conversion Time, First Conversion	2, 5	+25°C	-	$4t_{CLK}$+0.63	µs
			+125°C, -55°C	-	$4t_{CLK}$+0.8	µs
t_{ALEW}	ALE Pulse Width	5	+25°C	30	-	ns
			+125°C, -55°C	50	-	ns
t_{AS}	Address Setup Time	5	+25°C	40	-	ns
			+125°C, -55°C	80	-	ns
t_{AH}	Address Hold Time	5	+25°C	0	-	ns
			+125°C, -55°C	0	-	ns
t_{WRL}	$\overline{WR}$ Pulse Width	5	+25°C	100	$t_{CLK}/2$	ns
			+125°C, -55°C	100	$t_{CLK}/2$	ns
t_{WREOC}	$\overline{WR}$ to EOC Low	2, 4, 5	+25°C	-	130	ns
			+125°C, -55°C	-	160	ns
t_{HOLD}	$\overline{WR}$ to $\overline{HOLD}$ Delay	2, 5	+25°C4	-	150	ns
			+125°C, -55°C	-	170	ns
t_{CKHR}	Clock to $\overline{HOLD}$ Rise Delay	2, 5	+25°C	150	450	ns
			+125°C, -55°C	120	500	ns
t_{CKHF}	Clock to $\overline{HOLD}$ Fall Delay	3, 5	+25°C	50	200	ns
			+125°C, -55°C	40	225	ns
t_{CKEOC}	Clock to EOC High	2, 5	+25°C		630	ns
			+125°C, -55°C		800	ns
t_{DATA}	to DATA change	3, 5	+25°C	100	350	ns
			+125°C, -55°C	90	400	ns
t_{CD}	$\overline{CS}$ to DATA	5	+25°C	-	70	ns
			+125°C, -55°C	-	85	ns
t_{AD}	HBE to DATA	5	+25°C	-	50	ns
			+125°C, -55°C	-	70	ns
t_{RD}	$\overline{RD}$ LO to Active	5, 7	+25°C	-	100	ns
			+125°C, -55°C	-	125	ns
t_{RX}	$\overline{RD}$ HI to Inactive	5, 8	+25°C	-	60	ns
			+125°C, -55°C	-	70	ns

TABLE 3. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V+ = 5V, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz with $t_R = t_F \leq 25$ns and 50% Duty Cycle, Unless Otherwise Specified.

SYMBOL	PARAMETER	NOTES	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
t_R	Output Rise Time	5, 6	+25°C	-	40	ns
			+125°C, -55°C	-	60	ns
t_F	Output Fall Time	5, 6	+25°C	-	30	ns
			+125°C, -55°C	-	50	ns

NOTES:

2. Slow memory mode timing.
3. Fast memory or DMA mode of operation, except the first conversion which is equal to t_{CONV}.
4. Maximum specification to prevent multiple triggering with .
5. All input drive signal are specified with tr = tf ≤ 10ns and shall swing from 0.4V to 2.4V for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except tRD & tRX).
6. t_R and t_F load is C_L = 100pF (including stray capacitance) to DG and is measured from the 10% - 90% point.
7. t_{RD} is the time required for the data output level to change by 10% in response to crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with R_L = 2.5KΩ and C_L=10pF (including stray to DG).
8. t_{RX} is the time required for the data output level to change by 10% in response to crossing a voltage level of 1.4V. V_{OL} to High-Z is measured with R_L = 2.5KΩ to V+ and C_L = 10pF (including stray to DG).
9. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
10. Functionality is guaranteed by negative gain error test to ±4LSB.
11. Applies to all outputs which three state.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-IN)	1, 7, 9
Final Electrical Test Parameters	1*, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A Test Requirements	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D Endpoints	1, 7, 9

* PDA applies to Subgroup 1 only. No other subgroups are included in PDA

Timing Waveforms

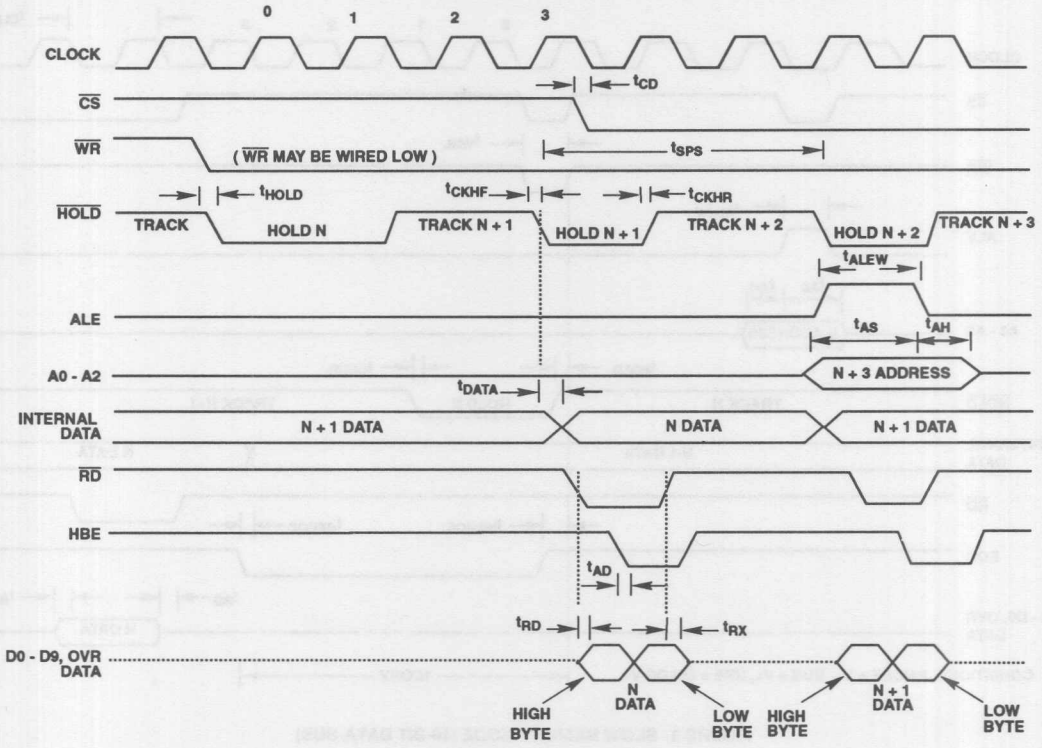
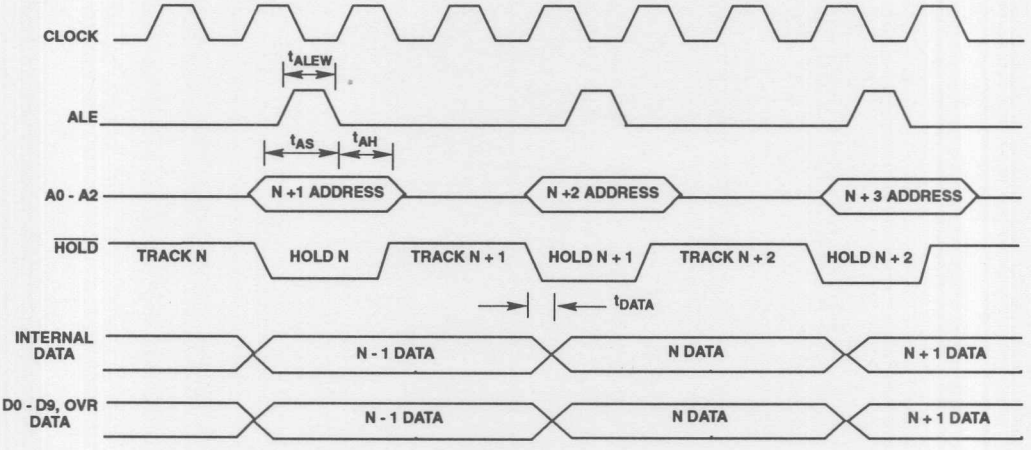


FIGURE 1. FAST MEMORY MODE (8-BIT DATA BUS)



CONDITIONS: SMODE = V+, $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = DG, BUS = V+, HBE = DG OR V+

NOTE: ECO OUTPUT IS LOW CONTINUOUSLY.

FIGURE 2. DMA MODE (16-BIT DATA BUS)

Timing Waveforms (Continued)

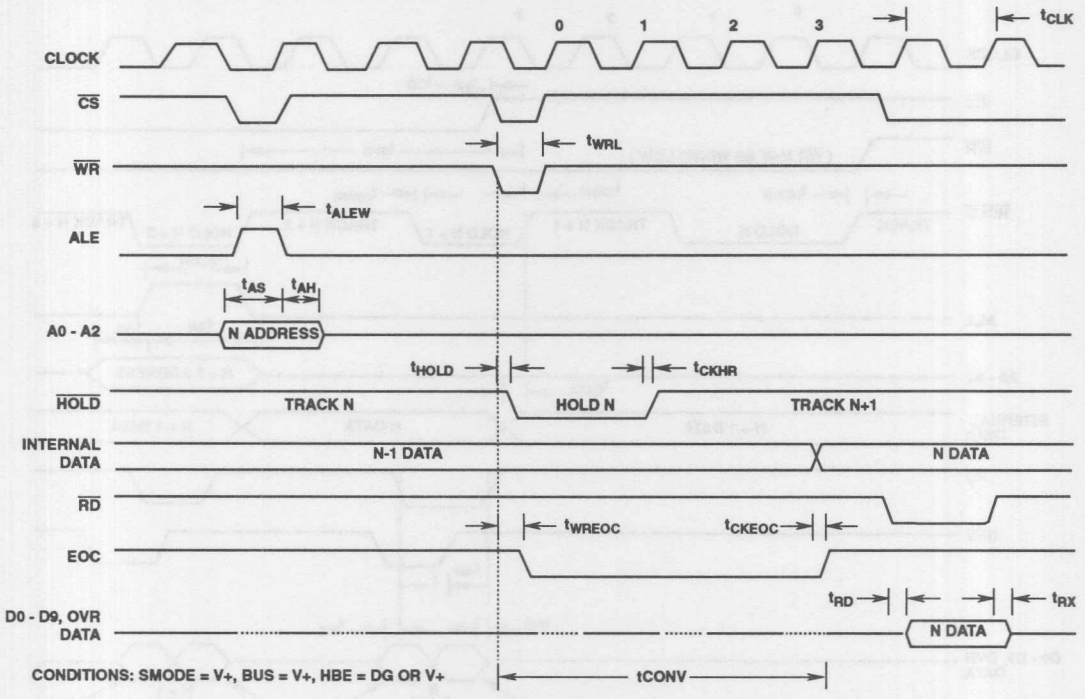
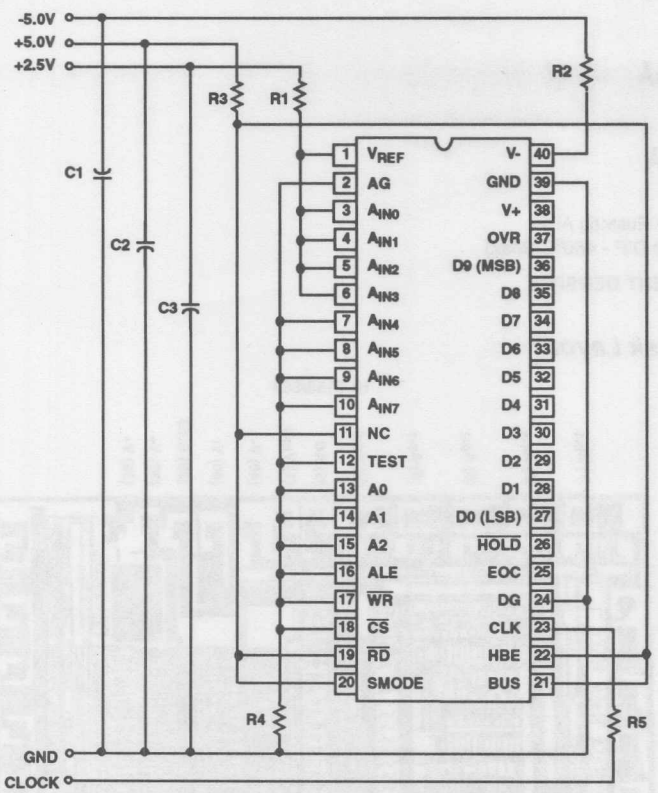


FIGURE 3. SLOW MEMORY MODE (16-BIT DATA BUS)

Burn-In Circuit

HI-7153/883 CERAMIC DIP



NOTES:

R1, R4, R5 = 1kΩ ±5%, 0.25W (Min)
R2, R3 = 100Ω, ±5%, 0.25W (Min)
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2
C1 - C3 = 4.7µF, ±20%
CLOCK = 450kHz (±50kHz) Square Wave With
50% Duty Cycle (±20%), 0V to 2.5V

Metallization Topology

DIE DIMENSIONS:
179 x 212 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

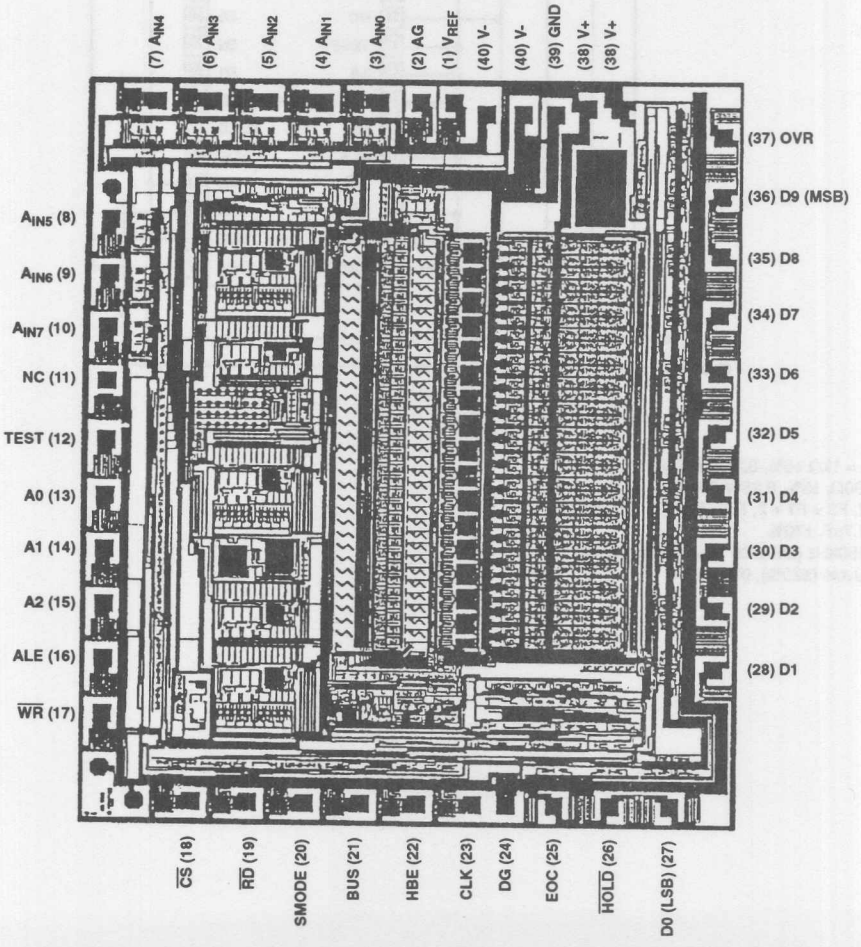
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP - 460°C (Max)

WORST CASE CURRENT DENSITY:
2.5×10^4 A/cm^2

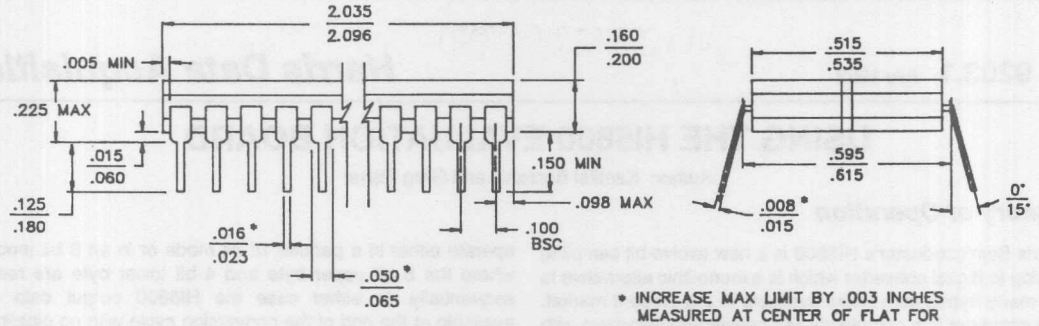
Metallization Mask Layout

HI-7153/883



Packaging†

40 PIN CERAMIC DIP



* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510-D-5

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes and Dimensions

Harris Semiconductor

APPNOTE

No. 9203.1 July 1992

Harris Data Acquisition

USING THE HI5800 EVALUATION BOARD

Author: Kantilal Bacrania and Greg Fisher

Theory of Operation

Harris Semiconductor's HI5800 is a new twelve bit sampling analog to digital converter which is a monolithic alternative to the many hybrid converters available in the present market. The converter is a completely self-contained subsystem with a sample and hold, a curvature corrected band-gap voltage reference, controller, a 7 bit flash converter, a 14 bit accurate D/A converter (DAC), wide-band gain amplifier, timing generator and I/O drivers. It is designed for applications where high speed and wide bandwidth are essential. It has a conversion time of ~200ns (5MHz) with a throughput rate of 330ns (3MHz). The 12 bit performance is guaranteed over temperature with no missing codes.

The HI5800 is powered by +5V and -5V supplies with an input range of -2.5V to +2.5V. Separate chip select and convert command pins are provided to allow convenient addressing in multiple converter systems. The 12 bit three state output is formatted as offset binary with an overflow bit. The overflow bit indicates over and underflow conditions by a logic high state. The 12 output bits all remain at logic high states for overflow and logic low states for underflow conditions. The digital output bus can be configured to operate either in a parallel 12 bit mode or in an 8 bit mode where the 8 bit upper byte and 4 bit lower byte are read sequentially. In either case the HI5800 output data is available at the end of the conversion cycle with no pipeline delay or latency. Valid data on the output bus is indicated by the logic state of the interrupt request output pin. The converter has fully TTL compatible input buffers for the digital control pins and also has TTL compatible BiCMOS output drivers. The output drivers can drive capacitive loads in excess of 100pF and do not require external data registers for interfacing to a data bus. The converter allows use of the internal +2.5V reference or an external reference through separate reference output and reference input pins. The voltage appearing on the reference input pin REF_{IN} is inverted by an internal amplifier to provide the bipolar input range. The sample and hold offset can be externally adjusted through the use of 2 offset pins if desired. External adjustments to the ADC gain at the +2.5V and -2.5V ends of the input range are also possible through 2 additional pins provided.

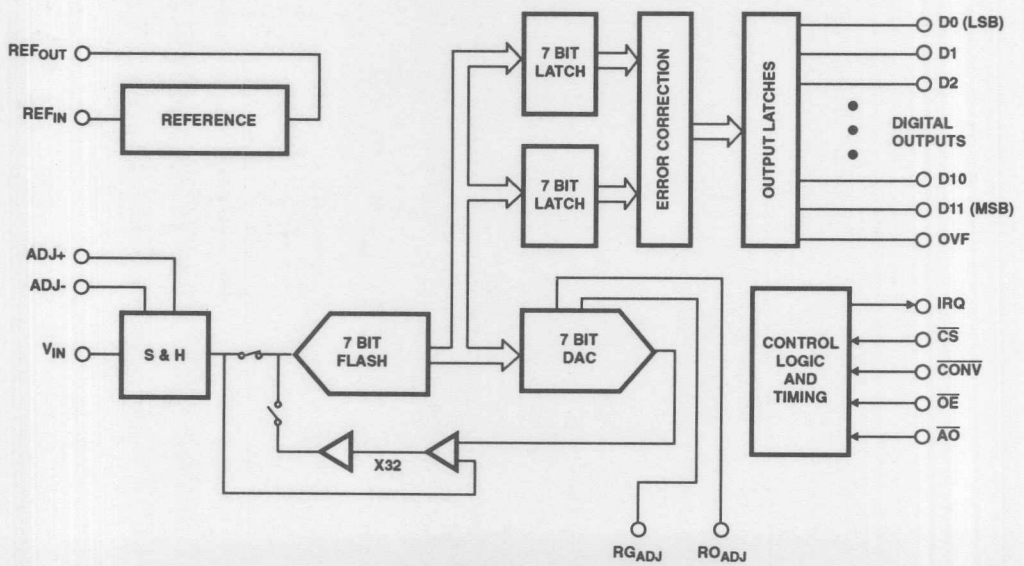


FIGURE 1. HI5800 BLOCK DIAGRAM

The HI5800 is a sampling converter which uses a two step subranging conversion technique with digital error correction. A block diagram illustrating the architecture is shown in Figure 1. The converter uses a high input impedance (>10MΩ) sample and hold at the front end. During the first pass of the two step conversion process, the sample and hold output is connected through a switch to a seven bit bipolar flash analog to digital converter. The flash converter digitizes the sample and hold output and feeds the result to the 7 bit digital to analog converter and to a 7 bit high byte latch. The output of the DAC, which uses thin film laser trimmed resistors to achieve 14 bit accuracy, is subtracted from the output of the sample and hold amplifier and the difference is amplified by a gain of 32. The gain of 32 is realized by two cascaded wide bandwidth op amps. The output of the second amplifier is now connected through the switch to the input of the flash converter for the second pass through the flash. This marks the second step of the two step conversion process. The flash converter second pass output is then fed to a seven bit latch which stores the low byte. The error correction logic takes the two 7 bit words from the high and low byte latches and computes the final twelve bit word with overflow detection. The output data is stored in latches which drive tristate output buffers.

The HI5800 is controlled with four digital pins: chip select ($\overline{CS}$), convert ($\overline{CONV}$), Output Enable ($\overline{OE}$) and an output byte select ($\overline{A0}$). Figure 2 shows the functional timing diagram for $\overline{CS}$, $\overline{CONV}$, and $\overline{OE}$ and the output bits D11-D0, OVF and output pin IRQ. The $\overline{CS}$ pin enables the converter when held low. When $\overline{CS}$ is held high, the output bits are tristated and the converter ignores the states of the other digital control pins. When $\overline{CS}$ is held low, the $\overline{CONV}$ pin starts the conversion with a negative going edge. In Figure 2, the converter is enabled by driving $\overline{CS}$ low at time t0 and a conversion is started by driving $\overline{CONV}$ low at time t1. The converter is disabled with all output bits tristated when $\overline{CS}$ is held high as shown at times t0 and t5. If the $\overline{CONV}$ pin is held low after an initial negative going edge, then the converter will operate in a continuous convert mode with a self timed sample rate of just over 3MHz. For a synchronous sampling system, the $\overline{CONV}$ pin can be driven by an externally derived system clock at sampling rates of up to 3MHz. Once the conversion is started, the converter's controller and timing logic control the entire conversion process until both the present conversion and the next sample and hold acquisition time are complete. At this time, approximately 333ns after the start of the conversion, the next falling edge of the $\overline{CONV}$ pin will be recognized and a new conversion started. The Interrupt ReQuest (IRQ) pin allows the user to monitor the conversion process. This signal goes high upon the start of a conversion for about 200ns indicating that the converter is busy with the conversion. The falling edge of the IRQ pin, at time t2 in Figure 2, indicates that the new data is present on the output bus. The converter provides the new data at the end of the current conversion cycle without any pipeline delays. This feature is extremely valuable in continuous servo applications when pipeline latency cannot be tolerated. The output enable pin $\overline{OE}$ allows the output drivers to be switched between the tristate mode and the data valid mode when the chip is selected. All output pins except for IRQ are tristated with this function. This function is illustrated at time t3 and t4 in Figure 2. The output bus can be switched between the tristate and driven modes at any time during the conversion cycle.

A byte select pin ($\overline{A0}$) allows eight bit processors to read the data bus without any need for external logic. The 12 bit output word can be formatted either in a 12 bit parallel mode or in an 8 bit mode with the upper and lower bytes read sequentially. With $\overline{A0}$ held low, the 12 data bits will appear on the data pins D11-D0. This is shown in Figure 3 at time t1. Time t2 in Figure 3 shows that when $\overline{A0}$ is held high, the data pins D11-D4 will now output the data bits D3-D0 followed by 4 trailing zeroes. The data bits D3-D0 still remain on the lower data pins D3-D0. Thus an 8 bit bus can read the 12 bit word through the pins D11-D4 by toggling the $\overline{A0}$ control pin.

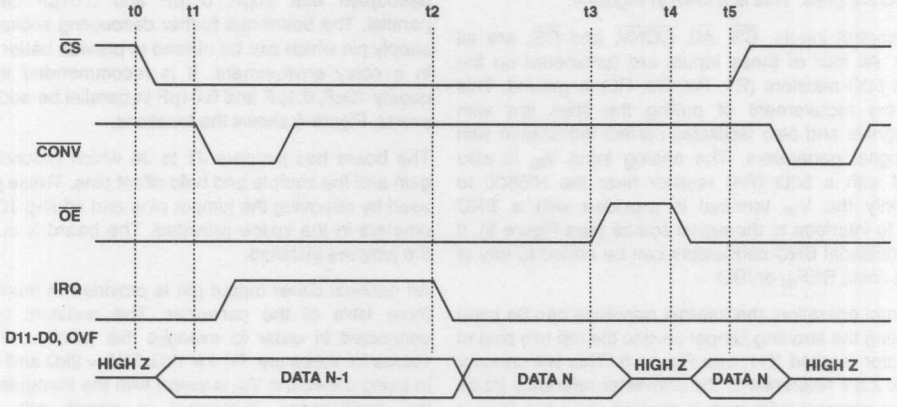


FIGURE 2. HI5800 FUNCTIONAL TIMING DIAGRAM

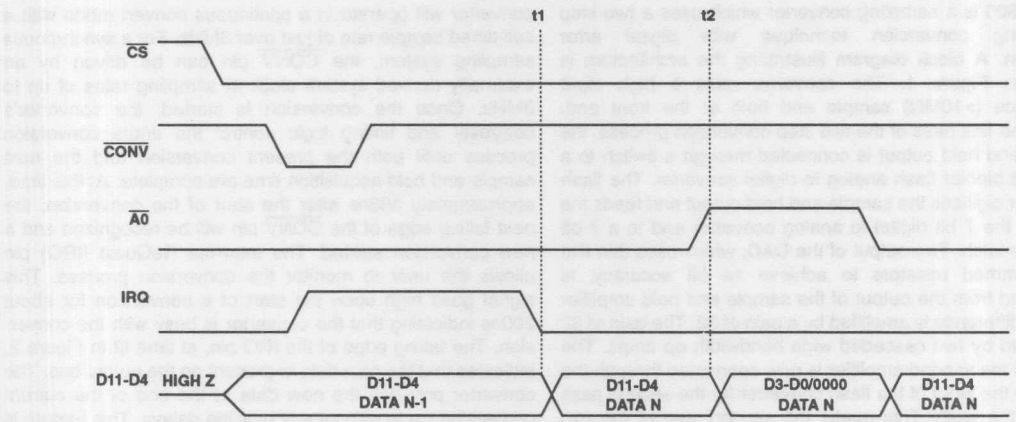


FIGURE 3. HI5800 DATA BYTE SELECT DIAGRAM

Description of the Evaluation Board

The evaluation board for the HI5800 is a three layer printed circuit board specifically designed to facilitate quick evaluation of the part. The board as supplied has been fitted with the minimum number of passive components needed to insure low noise functionality of the converter. The I/O can be accessed through a 50 pin ribbon cable connector. All signals except the V_{IN} (analog signal input) and the REF_{IN} (External Reference input) are brought out on the edge connector.

Getting Started

In order to minimize lead inductance, make sure the supply pins and ground are doubly connected on the edge connector. For the ease of use the HI5800 analog and digital power supply pins are wired together on the board and do not require separation for the evaluation board. If desired, the supplies can be hooked up with external wires to the pins marked VEE, VCC and GND with up to 16 gauge wire going to regulated supplies. This is shown in Figure 4.

The four control inputs, $\overline{CS}$, $\overline{A0}$, $\overline{CONV}$, and $\overline{OE}$, are all active low. All four of these inputs are terminated on the board with 50Ω resistors (R1, R2, R3, R5) to ground. This removes the requirement of pulling the lines low with external signals and also facilitates correct termination with external signal generators. The analog input V_{IN} is also terminated with a 50Ω (R4) resistor near the HI5800 to ground. Only the V_{IN} terminal is provided with a BNC connector to interface to the signal source (see Figure 5). If desired, additional BNC connectors can be added to any of the control lines, REF_{IN} or IRQ.

Under normal operation, the internal reference can be used by connecting the shorting jumper plug to the top two pins of the connector marked X11, see Figure 5. This will connect the internal 2.5V reference to the converter reference input. If use of an external reference is desired, then the jumper plug should be connected to the bottom two pins and the external reference is fed to the REF_{IN} pin on the board.

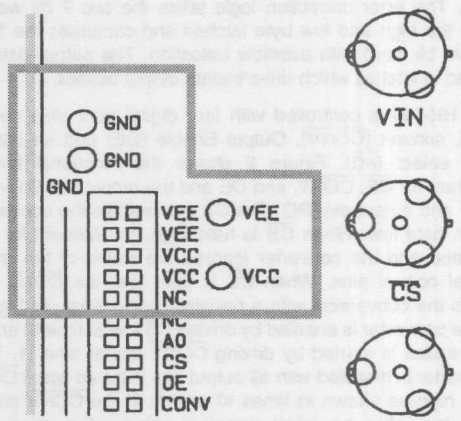


FIGURE 4.

The reference and three of the power supply points are decoupled with 10µF, 0.1µF and 0.01µF capacitors in parallel. The board has further decoupling sockets on every supply pin which can be utilized to provide better decoupling in a noisy environment. It is recommended that a good quality 10µF, 0.1µF and 0.01µF in parallel be added to these points. Figure 6 shows the locations.

The board has jumpers J1 to J4 which ground the offset, gain and the sample and hold offset pins. These pins can be used by removing the jumper pins and adding 10kΩ potentiometers in the space provided. The board is supplied with the jumpers installed.

An optional dither output pin is provided to monitor the last three lsb's of the converter. The resistors need to be connected in order to exercise this function. The resistor values for these are: R14 = 1kΩ, R12 = 2kΩ and R13 = 4kΩ. In using dither, the V_{IN} is swept with the triangular wave and the oscilloscope X-channel is swept with the same waveform. The Y-channel is connected to the dither out pin. The resultant waveform is shown in Figure 8.

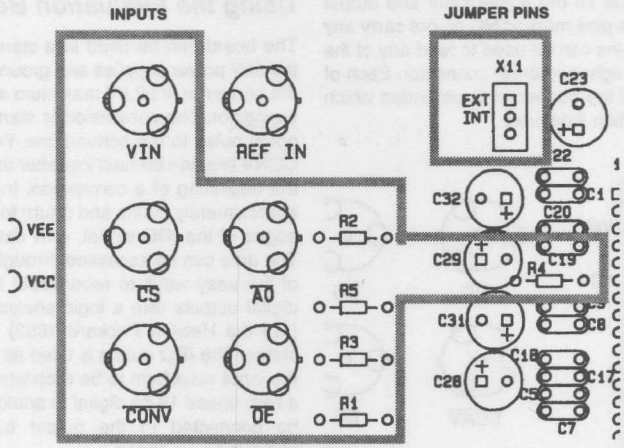


FIGURE 5.

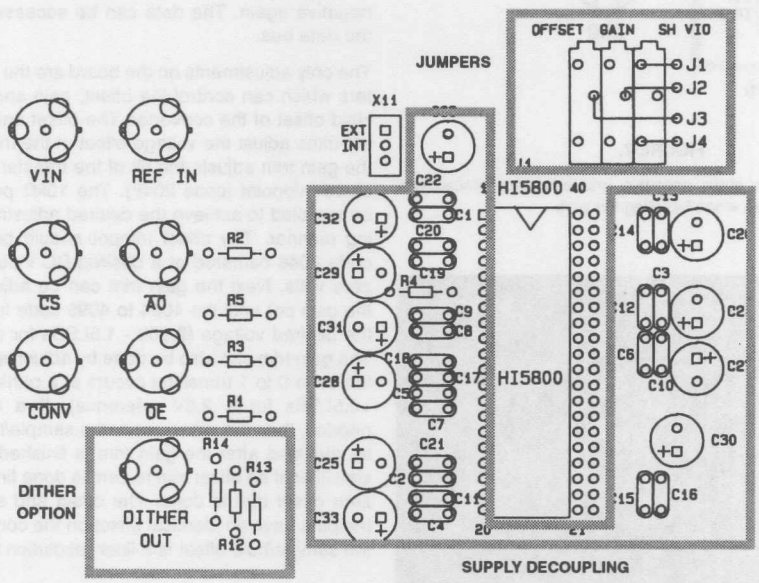


FIGURE 6.

The edge connector carries all the digital input and output signals (see Figure 7). The pins marked NC do not carry any signals. If desired, these pins can be used to feed any of the other pins that are not brought out to the connector. Each of the pins on the left side of the connector is grounded which allows convenient termination if desired.

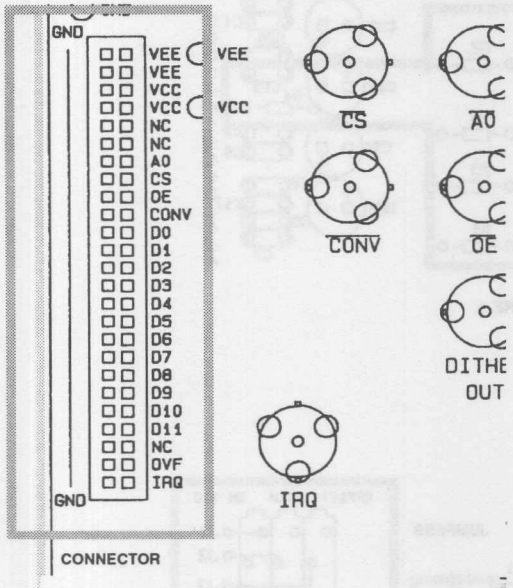


FIGURE 7.

NOTE: The device is static sensitive and adequate precautions should be taken when handling the part.

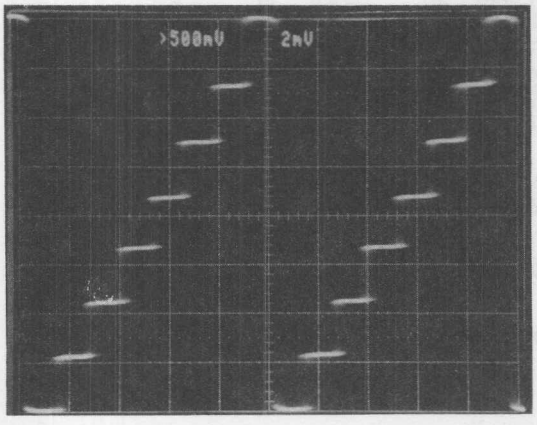


FIGURE 8.

Using the Evaluation Board

The board can be used in a stand alone mode. Make sure the ±5V power supplies and ground are present. The input to the converter is ±2.5V maximum and is connected to the V_{IN} connector. The conversion is started by applying a negative going pulse to the convert line. For continuous convert, the $\overline{CONV}$ line can be held low after the first transition to zero. At the beginning of a conversion, the IRQ line will go high for approximately 200ns and return to zero. At each of the falling edges of the IRQ signal, new data is available on the bus. The data can be accessed through the edge connector. One of the easy ways to reconstruct the data is by reading the digital outputs with a logic analyzer with charting capability (like the Hewlett Packard 1652) and observing the output states. The IRQ output is used as clock qualifier. This allows the input waveform to be reconstructed and displayed. Also, a high speed 12-bit digital to analog converter (HI-562A) can be connected to the output bus and the DAC output observed on a scope.

The converter can also be used in a triggered mode where the $\overline{CONV}$ pulse is a negative going pulse with a pulse width of 25ns to 300ns and period of ≥330ns. Again, at each start of conversion, the IRQ will go high for ~200ns. The $\overline{CONV}$ pulse should go high before the end of the acquisition period which is ~100ns after the IRQ goes low. In order to start a new conversion, the $\overline{CONV}$ line should go negative again. The data can be accessed at any time on the data bus.

The only adjustments on the board are the three potentiometers which can control the offset, gain and the Sample and Hold offset of the converter. The offset and sample/hold offset trims adjust the voltage offset of the transfer curve while the gain trim adjusts the tilt of the transfer curve around the curve midpoint (code 2048). The 10kΩ potentiometers can be installed to achieve the desired adjustment in the following manner. The offset trimpot should be adjusted to get code 2048 centered at a desired DC input voltage such as zero volts. Next the gain trim can be adjusted by trimming the gain pot until the 4094 to 4095 code transition occurs at the desired voltage (2.500 - 1.5LSBs for a 2.5V reference). The gain trim can also be done by adjusting the gain pot until the code 0 to 1 transition occurs at a particular voltage (-2.5 +0.5LSBs for a 2.5V reference). If a nonzero offset is needed, then the offset pot or the sample/hold offset pot can be adjusted after the gain trim is finished. The gain trim is simplified if an offset trim to zero is done first and then a nonzero offset trim is done. The offset and sample/hold offset trimpots have an identical effect on the converter except that the sample/hold offset is a finer resolution trim.

Pin Description and Typical Evaluation Data

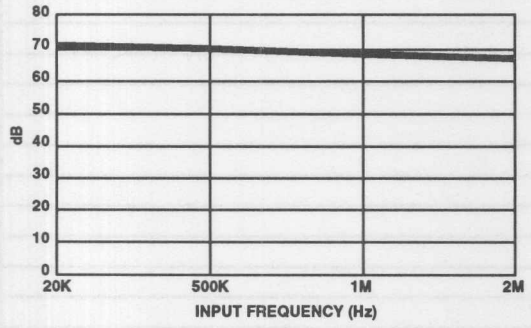
The pin description is presented in Table 1. This is followed by some evaluation curves on typical performance of HI5800.

TABLE 1. PIN DESCRIPTION

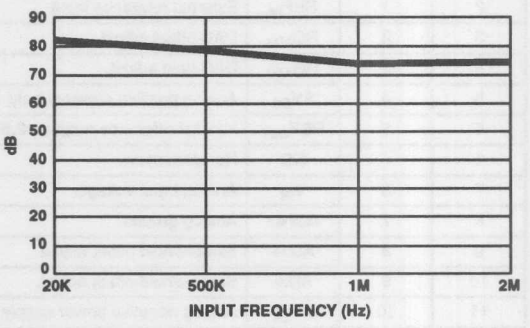
44 PIN PLCC	40 PIN CERDIP	PIN NAME	PIN DESCRIPTION
2	1	REF_{IN}	External reference input.
3	2	RO_{ADJ}	DAC offset adjust.
4	3	RG_{ADJ}	DAC gain adjust.
5	4	AV_{CC}	Analog positive power supply, +5V
6	5	REF_{OUT}	Internal reference output, +2.5V.
1	--	NC	No connection.
7	6	V_{IN}	Analog input voltage.
8	7	AGND	Analog ground.
9	8	ADJ+	Sample/hold offset adjust.
10	9	ADJ-	Sample/hold offset adjust.
11	10	AV_{EE}	Analog negative power supply, -5V
13	11	AV_{CC}	Analog positive power supply, +5V
14	12	AGND	Analog ground.
15	13	AV_{EE}	Analog negative power supply, -5V
16	14	$\overline{A0}$	Output byte control input, active low. When low, data is presented as a 12 bit word or the upper byte (D11-D4) in 8 bit mode. When high, the second byte contains the lower LSB's (D3-D0) with 4 trailing zeroes. See Text.
17	15	$\overline{CS}$	Chip Select input, active low. Dominates all control inputs.
12	--	NC	No connection.
18	16	OE	Output Enable input, active low.
19	17	$\overline{CONV}$	Convert start input. Initiates conversion on the falling edge. If held low, continuous conversion mode overrides and remains in effect until the input goes high.
20	18	DV_{EE}	Digital negative power supply, -5V.
21	19	DGND	Digital ground.
22	20	DV_{CC}	Digital positive power supply, +5V.
24	21	AV_{CC}	Analog positive power supply, +5V.
25	22	D0	Data bit 0, (LSB).
26	23	D1	Data bit 1.
27	24	D2	Data bit 2.
28	25	D3	Data bit 3.
23	--	NC	No connection
29	26	D4	Data bit 4.
30	27	D5	Data bit 5.
31	28	D6	Data bit 6.
32	29	D7	Data bit 7.
33	30	AV_{EE}	Analog negative power supply, -5V.
35	31	AGND	Analog ground.
36	32	DGND	Digital ground.
37	33	DV_{CC}	Digital positive power supply, +5V.
38	34	D8	Data bit 8.
39	35	D9	Data bit 9.
34	-	NC	No connection.
40	36	D10	Data bit 10.
41	37	D11	Data bit 11 (MSB).
42	38	AV_{CC}	Analog positive power supply, +5V.
43	39	OVF	Overflow output. Active high when either an overrange or underrange analog input conditions is detected.
44	40	IRQ	Interrupt ReQuest output. Goes low when a conversion is complete.

Typical Performance Curves

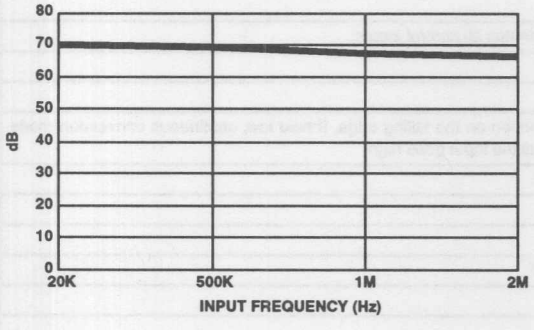
TYPICAL SNR vs INPUT FREQUENCY



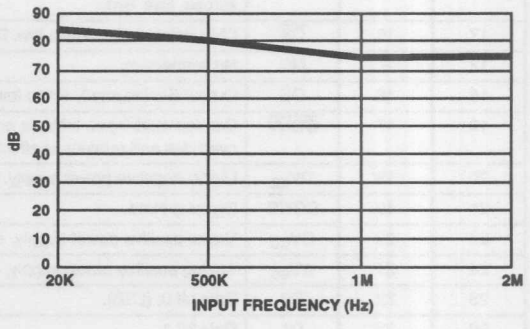
TYPICAL THD vs INPUT FREQUENCY



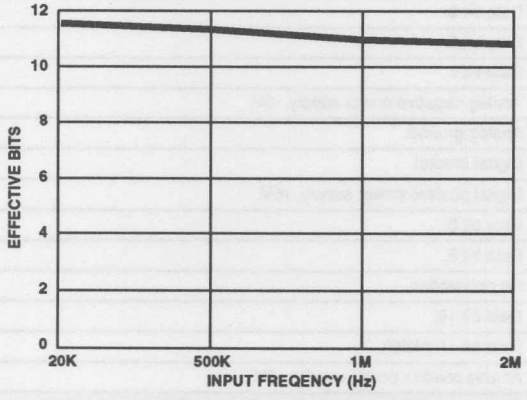
TYPICAL SND vs INPUT FREQUENCY



TYPICAL SPDF vs INPUT FREQUENCY

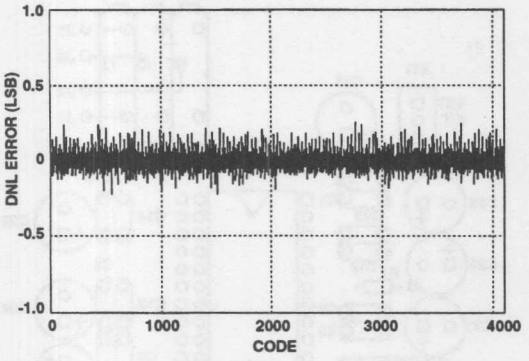


TYPICAL EFFECTIVE BITS vs INPUT FREQUENCY

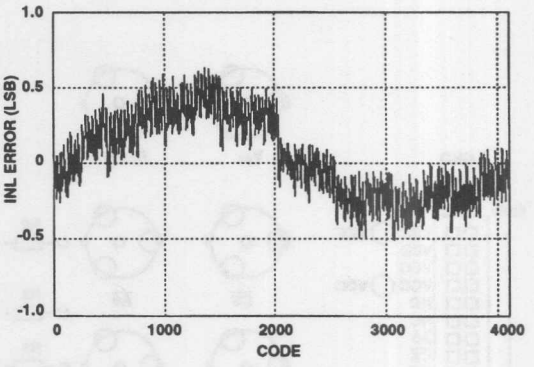


Typical Performance Curves (Continued)

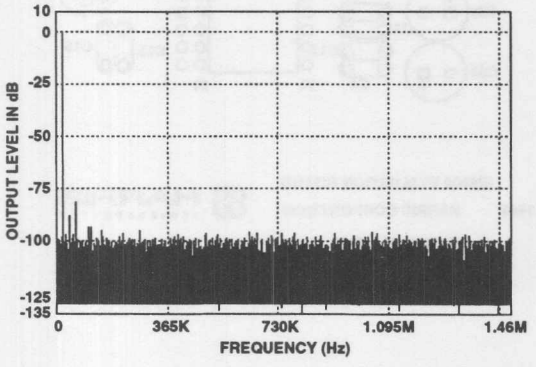
DIFFERENTIAL NON-LINEARITY



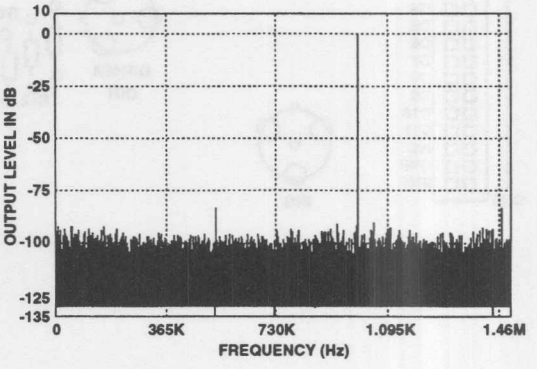
INTEGRAL NON-LINEARITY



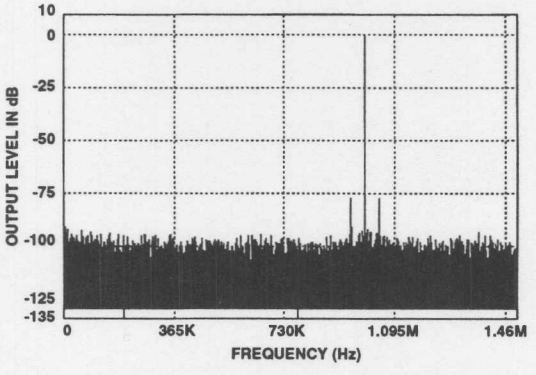
FFT SPECTRAL PLOT FOR F_{IN} = 20kHz, F_S = 3MHz



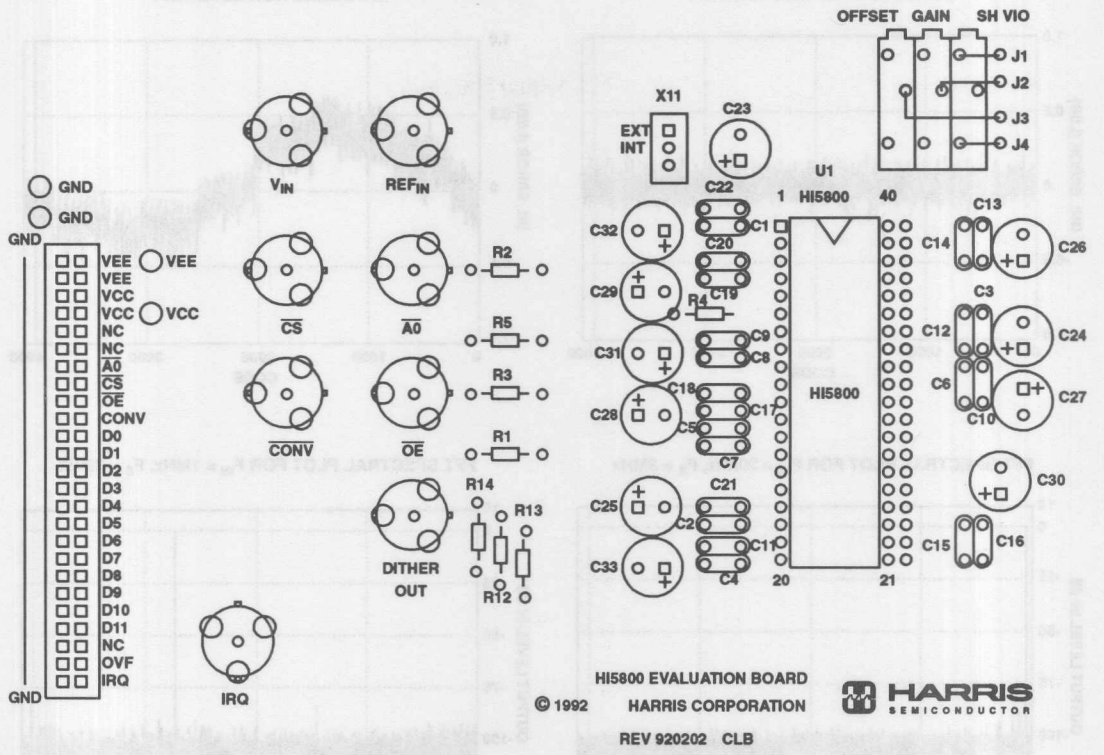
FFT SPECTRAL PLOT FOR F_{IN} = 1MHz, F_S = 3MHz



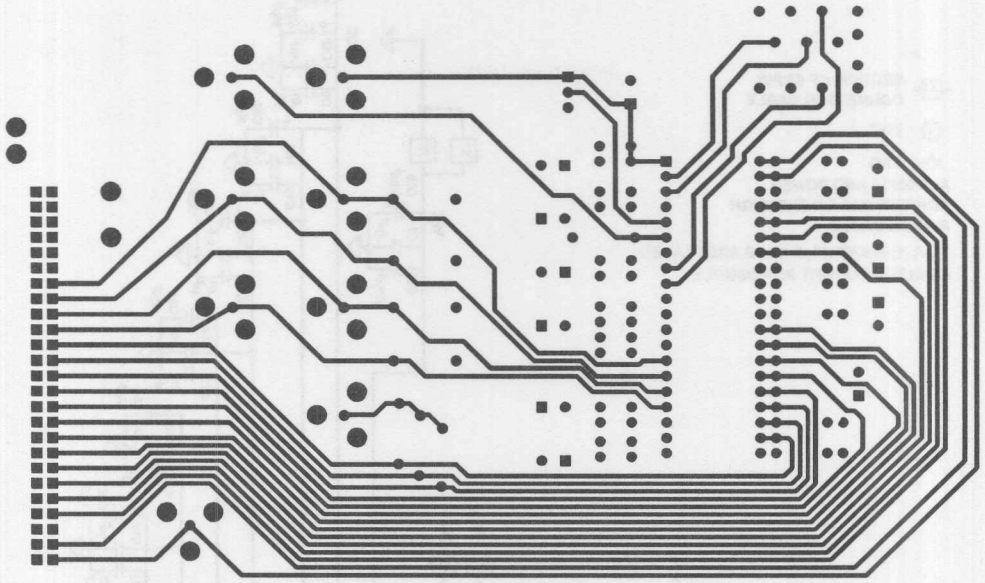
FFT SPECTRAL PLOT FOR F_{IN} = 2MHz, F_S = 3MH



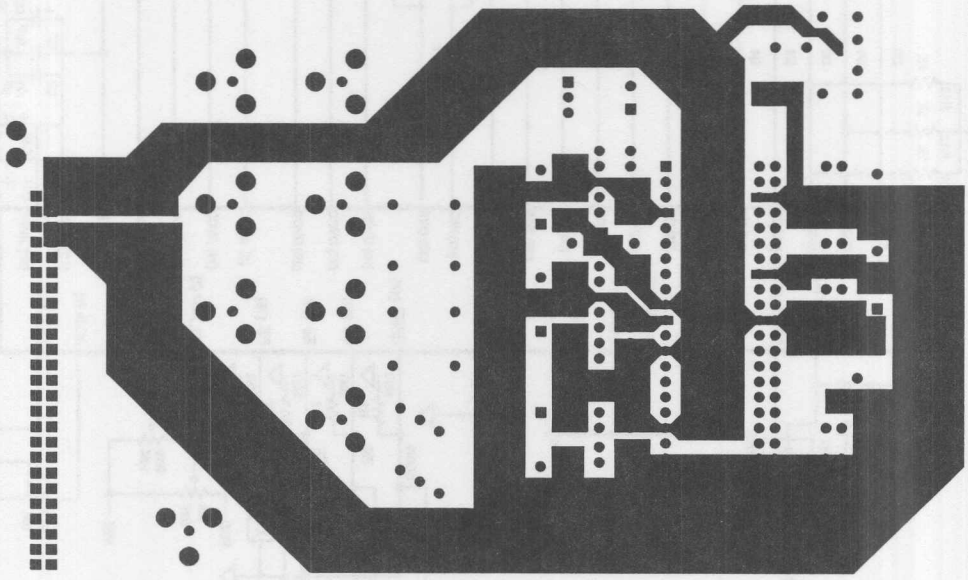
Silk Screen


OFFSET GAIN SH VIO
J1
J2
J3
J4
X11
EXT
INT
C23
U1
1 HI5800 40
C22
C1
C20
C19
R4
C9
C8
C18
C17
C5
C7
C21
C2
C11
C4
20
21
HI5800
C32
C29
C31
C28
C25
C33
C13
C14
C26
C3
C12
C24
C6
C27
C10
C30
C15
C16
R2
R5
R3
R1
R14
R13
R12
GND
GND
GND
VEE
VEE
VCC
VCC
NC
NC
A0
CS
OE
CONV
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
NC
OVF
IRQ
GND
VEE
VCC
VIN
REFIN
CS
A0
CONV
OE
DITHER
OUT
IRQ
HI5800 EVALUATION BOARD
© 1992 HARRIS CORPORATION
REV 920202 CLB
HARRIS
SEMICONDUCTOR

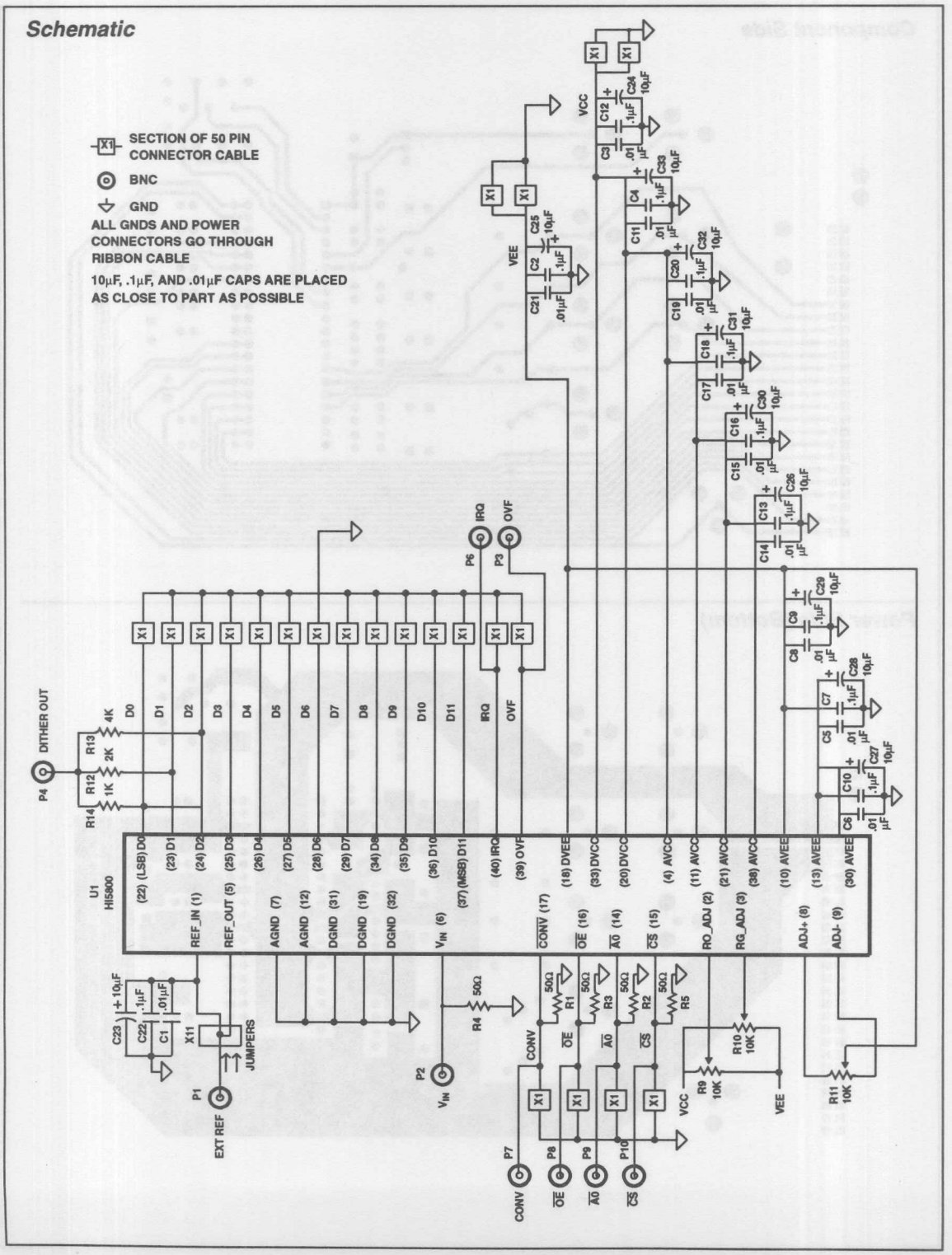
Component Side



Power Side (Bottom)



Schematic


SECTION OF 50 PIN CONNECTOR CABLE
BNC
GND
ALL GNDS AND POWER CONNECTORS GO THROUGH RIBBON CABLE
10µF, .1µF, AND .01µF CAPS ARE PLACED AS CLOSE TO PART AS POSSIBLE
U1
HI5800
DITHER OUT
EXT REF
JUMPERS
VCC
VEE
IRQ
OVF
CONV
AGND
DGND
REF_IN
REF_OUT
RO_ADJ
RG_ADJ
ADJ+
ADJ-
DVEE
DVCC
AVCC
AVEE

Materials List

Program : PC-FORM VERSION 5.10
Date : Apr 21 1992
Time : 01:07:27 PM
File In : 5800D.PNL
File Out : 5800D. MAT
Format : P-CAD MATERIALS LIST

ITEM	QTY	PART NAME	REFERENCE DESIGNATOR	DESCRIPTION
1	11	CK06	C1, C3, C5, C6, C8, C11, C14, C15, C17, C19, C21	VAL = .01µF
2	11	CK06	C4, C7, C9, C10, C12, C13, C16, C18, C20, C2, C22	VAL = .1µF
3	5	RC05	R2, R3, R5, R1, R4	VAL = 50Ω
4	1	RC05	R12	VAL = 2K
5	1	RC05	R13	VAL = 4K
6	1	RC05	R14	VAL = 1K
7	1	50RCONGT	X1	50 PIN RIBBON CONNECTOR
8	11	PCAP	C24, C25, C23, C26, C27, C28, C29, C30, C31, C32, C33	VAL = 10µF
9	3	TRMPOT	R11, R9, R10	VAL = 10K
10	8	RBNC	P1, P2, P3, P4, P6, P7, P8, P9, P10	
11	1	3PINJUMP	X11	
12	1	HI5800	U1	